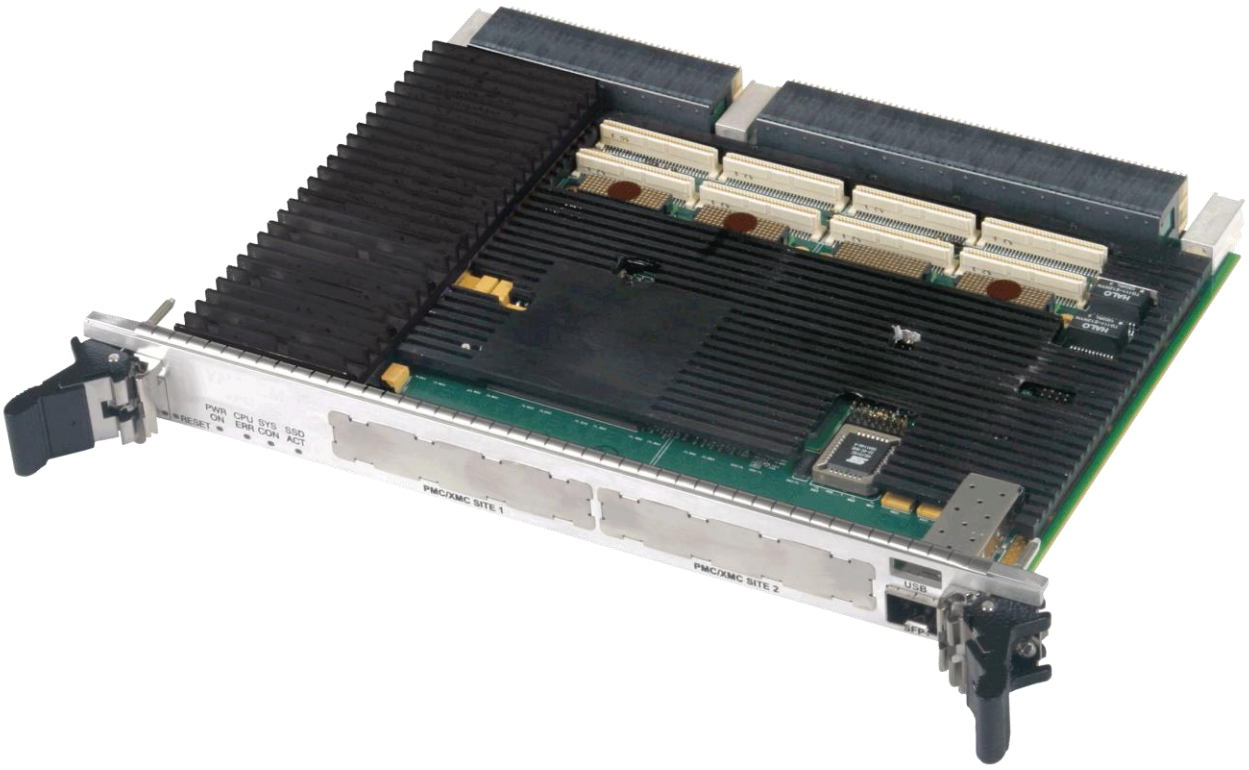
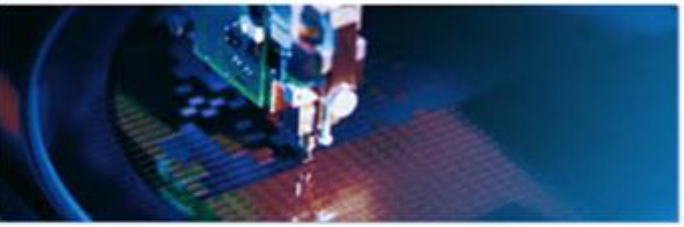
USER MANUAL





CPU-111-10 (VPQ)
Intel Xeon Quad-Core 6U VPX Single Board Computer

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Dynatem
A member of Eurotech Group

CPU-111-10 User's Manual Rev. Draft 0.1

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Dynatem
23263 Madero, Suite C
Mission Viejo, CA 92691

Phone: (949) 855-3235

Fax: (949) 770-3481

www.dynatem.com

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1. Features

The CPU-111-10 is a rugged, high-performance 6U VPX (VITA 46) Single Board Computer (SBC) featuring a quad-core Intel L5408 Xeon processor and integrated 10 Gigabit Ethernet switch to support full-mesh backplane data layer interconnectivity for up to eight SBCs integrated into a single chassis. Available in air cooled or conduction cooled formats, the CPU-111-10 conforms to the OpenVPX (VITA 65) payload module profile MOD6-PAY-4F2T-12.2.2.4 with four fat pipes (10 GBase-BX4) and two thin pipes (1000Base-T).

Providing unparalleled data processing capabilities in a single-slot 6U VPX form factor card with built-in 10 Gigabit Ethernet fabric switching, the CPU-111-10 serves as an ideal open-architecture building-block for next-generation Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR) applications onboard (un)manned air / ground vehicles and shipboard platforms. Standard onboard I/O resources includes up to 8x 10 Gigabit Ethernet, 2x 1 Gigabit Ethernet, 4x SATA, 2x USB 2.0, 1x RS-232/485, and 1x VGA video ports. Dual XMC / PMC expansion module sites enable additional I/O expansion, including 10G XAUI lanes from each XMC card to the 10G switched fabric.

Features of the CPU-111-10 include:

OPENVPX COMPATIBLE:

- Rugged Single-Slot 6U Single Board Computer compatible with VITA 65 OpenVPX Payload Module Profile MOD6-PAY-4F2T-12.2.2.4 (4x 10GBase-BX4 Fat Pipes and 2x 1000Base-T Thin Pipes)

HIGH PERFORMANCE x86 CPU:

- 4-Core Intel Xeon L5408 Processor @ 2.13 GHz with 4GB of DDR2 RAM
- Linux, VxWorks, Windows, LynxOS, QNX, x86 RTOS Compatible
- 16 GB Bootable Solid State Flash Disk

10 GIGABIT SWITCH:

- Integrated 10 Gigabit Ethernet Packet Processor Provides Full-Mesh Data Layer Switch Fabric for Up to 8 SBCs without Use of Additional Switch Board (7 XAUI Ports to VPX Backplane, 1 SPF+ Port)
- 10 Gigabit XAUI Fabric Interfaces to Dual XMC Expansion Modules
- Front Panel SFP+ 10 Gigabit Port Supporting CX4 Copper and Fiber Applications for Chassis-to-Chassis and Rack-to-Rack Communications

I/O & EXPANSION:

- Network: Up to 8x 10 Gigabit Ethernet, 2x 1 Gigabit Ethernet
- Peripherals: 4x SATA, 2x USB 2.0, 1x RS-232/485, and 1x VGA Video
- Dual XMC / PMC Mezzanine Expansion Sites

RUGGED DESIGN:

- Designed to Meet MIL-STD-810 Environmental Conditions (Thermal, Shock, Vibration, Humidity, Altitude) and Stresses of VPX Chassis Injection/Ejection
- Air and Conduction Cooled Variants; Conductively Cooled Version Integrate Board Stiffeners and Wedge Locks for High Shock and Vibration Immunity/Efficient Thermal Transfer.

2. Related Documents

Listed below are documents that describe applicable standards, the processor and chipset, and the peripheral components used on the CPU-111-10. Either download from the Internet or contact your local distributor for copies of these documents. Many of the documents are confidential and may require execution of a non-disclosure agreement between the supplier and CPU-110-10 user.

2.1 Standards

- *VITA 20-2001 - Conduction Cooled PMC, R1.1, February 2005*
- *VITA 32-2003 - Processor PMC, R1.0, July 2003*
- *VITA 42.0-2005 - XMC Switched Mezzanine Card Baseline Standard, D0.29, September 2005*
- *VITA 42.3-2006 - XMC PCI Express Protocol Layer Standard, R1.0, June 2006*
- *VITA 42.6-200x - XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard, R0.911, January 2009*
- *VITA 46.0-2007 - VPX Baseline Standard, R1.2, April 2008*
- *VITA 46.4-2008 - PCI Express on VPX Fabric Connector, R6.00, March 2008*
- *VITA 46.7-2008 - Ethernet on VPX Fabric Connector, R0.05, October 2008*
- *VITA 46.9-2005 - PMC/XMC Pinout Mapping, R0.1, May 2005*
- *VITA 46.21-2009 - Distributed Switching on VPX, R0.01, February 2009*
- *IEEE P1386 - Common Mezzanine Card Family (CMC), D2.4a, March 2001*
- *IEEE P1386.1 - CMC Physical and Environmental Layers, D2.4, January 2001*
- *JEDEC 4.20.10 - PC2-6400/5300/4200/3200 Registered DIMM Design Specification, R3.98, January 2009*

2.2 Product Specifications, Component Data Sheets, and Design Guides

- *CPU-111-10 Data Sheet, October 3, 2011*
- *CPU-111-10 Schematic Diagram, R0.1, June 2009*
- *CPU-111-10 Bill of Materials, R0.1, June 2009*
- *Quad-Core Intel® Xeon® Processor 5400 Series Datasheet, Doc. No. 318589-005, August 2008*
- *Quad-Core Intel® Xeon® Processor L5408 Series in Embedded Applications Thermal/Mechanical Design Guidelines, Doc. No. 319133-001, April 2008*
- *Intel® 5100 Memory Controller Hub Chipset Datasheet, Doc. No. 318378-003U, July 2008*
- *Intel® 5100 Memory Controller Hub Chipset for Communications, Embedded, and Storage Applications Thermal/Mechanical Design Guide, Doc. No. 318676-003US, July 2008*
- *Intel® Xeon® Processor 5000 Sequence with Intel® 5100 Memory Controller Hub Chipset for Communications, Embedded, and Storage Applications Platform Design Guide, Doc. No. 352108-2.3, April 2009*
- *Intel® I/O Controller Hub 9 (ICH9) Family Datasheet, Doc. No. 316972-004, August 2008*
- *Debug Port Design Guide for UP/DP Systems, Doc. No. 313373-001, June 2006*
- *Intel® 82599 10 Gigabit Ethernet Controller Datasheet, R0.6, October 2008*
- *Intel® 82571 & 82572 Gigabit Ethernet Controller Datasheet, R2.0, December 2006*
- *82571EB/82572EI Gigabit Ethernet Controller Design Guide, Doc. No. 315337-002, February 2008*
- *Micron MT47H256M8 DDR2 SDRAM Data Sheet, Doc. No. 09005aef824f87b6, Rev. B, September 2008*
- *PLX Technology ExpressLane PEX 8624-AA 24-Lane/6-Port PCI Express Gen 2 Switch Data Book, Version 0.80, November 2007*
- *Tundra Tsi384 PCIe-to-PCI/X Bridge User Manual, Doc. No. 80E1000_MA001_08, July 2008*
- *Tundra Tsi384 Board Design Guidelines, Doc. No. 80E1000_AN004_04, July 2008*
- *Fulcrum Microsystems FocalPoint FM4000 24-Port 10G Ethernet Switch Datasheet, R2.1, May 2009*
- *Fulcrum Microsystems FocalPoint FM4212/FM3212 12-Port 10G Ethernet Switch Datasheet Addendum, R1.1, March 2008*
- *Netlogic Puma AEL2005 10Gbps SFP+ Transceiver Data Sheet, R1.2, December 2007*
- *Silicon Motion SM750 LynxExpress Mobile Multimedia Companion Chip Data Sheet, R0.1, June 12, 2009*
- *Silicon Motion SM2240 Serial ATA to IDE Bridge Data Sheet, R0.3, November 26, 2008*
- *Silego SLG505YC264B Clock Synthesizer Data Sheet, Doc. No. 000-0084505B-10, R1.0, April 2008*
- *IDT ICS9DB403D Quad Differential Clock Buffer Data Sheet, Rev. J, February 2009*
- *Intersil ISL6313B Two-Phase Buck PWM DCDC Controller Data Sheet, Doc. No. FN6809.0, November 2008*
- *Linear Technology LTM4616 Dual 8A Low-Vin DC/DC Module Data Sheet, Doc. No. LT 1108, Rev. A, 2008*
- *Lattice Semiconductor ispPAC-POWR1220AT8 Power Supply Monitor/Sequencer/Controller Data Sheet, Doc. No. DS1015, June 2008*

3. Hardware Description

3.1 Overview and Specifications

The block diagram of the CPU-111-10 is shown below. The sections that follow describe the major functional blocks of the CPU-111-10.

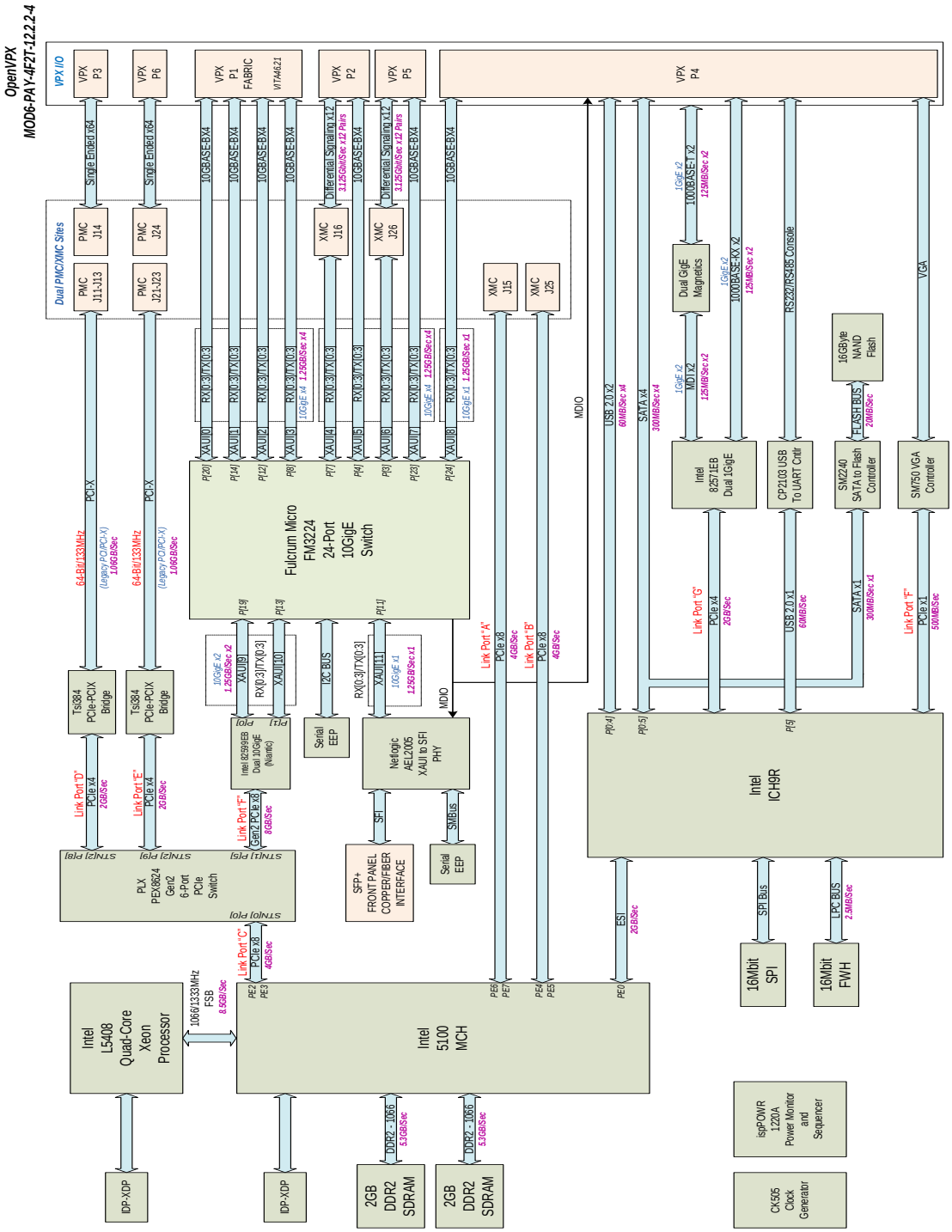


Figure 1: CPU-111-10 Block Diagram

Specifications

ARCHITECTURE	• 6U OpenVPX (ANSI/VITA 65); Compatible Profile: MOD6-PAY-4F2T- 12.2.2.4 - Payload board w/ Four Fat Pipes (10 GBase-BX4), Two 1000Base-T Thin Pipes (Control Plane)
OS SUPPORT	• Compatible with Linux, VxWorks, Windows, LynxOS, QNX, Other Popular x86 OS/Real Time Operation Systems (RTOS); Consult Factory for Available Drivers/BSPs
PROCESSOR	• Intel Xeon L5408 "Harpertown", 2.13 GHz Clockspeed, Quad-Core, Quad-Thread • 12 MB L2 Cache (Shared), 32 KB L1 Cache per Core, 1066 MHz Front Side Bus, 64-bit Instruction Set, 45-nm • Support for Intel 64, Virtualization, SpeedStep Technology
MEMORY	• System RAM Memory: 4GB DDR2 SDRAM at 533/667 MHz (1066 MHz DDR) • Bootable Onboard Flash SSD: 8GB Solid-State Disk (Soldered NAND Flash) • Firmware Hub: 16Mbit SPI Flash
CHIPSETS	• Intel 5100 Memory Controller Hub (MCH) • Intel ICH9R I/O Controller Hub (ICH) • Silicon Motion SM750 Graphic Processor Unit (GPU), 2D Graphics Acceleration • PLX PEX8624 Gen 2 PCI Express Switch • Tsi384 PCI Express to PCI-X Bridge • Intel 82599EB (Niantic) Dual 10-Gigabit Ethernet Controller (with IEEE-1588 Precision Time Protocol Support for sub-microsecond synchronization between node boards) • Intel 82571EB Dual 1 Gigabit Ethernet Controller • NetLogic Puma AEL2005 10GigE PHY/SerDes for SFP+ 10GBASE-LRM Requirements
ETHERNET SWITCH	• Fulcrum FM3224 10 Gigabit Ethernet Packet Processor for Layer 2 Switching • # Ports to VPX Backplane: up to 7x 10Gig Ethernet, 2x 1 Gigabit Ethernet • 1x Front Panel SFP+ Port Supporting 10 Gigabit Copper or Optical • Support for Full-Mesh Connectivity Between up to 8 CPU-111-10 SBCs • VITA 46.21 Full Mesh 10 Gigabit XAUI Interconnect for 5 Boards on Backplane per VITA 46.7 (Ethernet on VPX Fabric Connector) • Currently Unmanaged L2 Switch (Management Software Roadmapped – see below)
SWITCH MANAGMENT (Roadmapped)	Future Roadmapped Layer 2 and/or Layer 2 + Layer 3 Switch Management Software: • Managed L2 Switch Protocol Support: STP, RTSP, MSTP, LACP, GVRP, IGMP, SNMP Ethernet MIB, Remote Software Update and Administration (CLI / Web Browser) • Managed L2/L3 Switch Protocol Support: Protocols Mentioned Above + RIP, RIPng, OSPFv2, OSPFv3, BGP, ISIS, VRRP, SNMP MIB
XMC / PMC	• 2x XMC / PMC Mezzanine Sites for Front / Rear Panel I/O Expansion • PMC/XMC I/O routing as defined by VITA 46.9 • XAUI Fat-Pipe Connectivity from XMC to 10 Gig Switch • Busses: 64bit / 133MHz PCI-X, x8 PCIe
REAR I/O INTERFACES	• P0: VPX Utility Connectivity (per VITA 46.0) • P1: 4x 10Gig Ethernet (XAUI Fabric per VIA 46.21) • P2: XMC x12 Differential Pairs (per VITA 46.9), 1x 10Gig Ethernet XAUI from Switch • P3: PMC x64 Single Ended I/O (per VITA 46.9) • P4: 1x 10Gig Ethernet, 2x GigE Ethernet, 2x USB 2.0, 4x SATA 2.0, 1x RS-232/485, 1x VGA • P5: XMC x12 Differential Pairs (per VIA 46.9), 1x 10Gig Ethernet XAUI from Switch • P6: PMC x64 Single Ended I/O (per VITA 46.9)
FRONT PANEL	• 1x 10Gb Ethernet, SFP+ Copper or Optical
PHYSICAL	• Dimensions: 6U ANSI/VITA 46.0 VPX, Single-Slot, 1.0" Pitch • Weight: Approx. 3.0 lbs (<1350 grams) • Cooling: Conduction and Convection Cooling Options • Air Cooled Version: Includes Heatsinking and Aluminium Extraction Handles and Front Panel with Openings for Two PMC / XMC I/O • Conduction Cooled Version: Includes Heatspreaders,Wedge Locks, and Injector/Ejector Handles
POWER	• Power Input: +5 and +12 VDC • Power Consumption: 141W Typical (198 W Max)
ENVIRONMENTAL	Designed to Meet MIL-STD-810: • Operating Temperature: 0°C to +71°C (Air Cooled); -40°C to +77°C (Conduction Cooled) • Storage Temperature: -40°C to +85°C • Operating Humidity: 0 to 95%, Non-Condensing • Storage Humidity: 0 to 100%, Non-Condensing • Altitude: Unlimited with Proper Thermal Management • Random Vibration: 0.1 g/2 Hz 15-2 kHz, 3 Axes, 1 Hour/Axis • Shock: 40 g Peak, 11ms, 3 pos/neg per Axis, 36 Terminal Peak Sawtooth Pulses
RELIABILITY	• MTBF Per MIL-HDBK-217F: greater than XXXX hours

REAR TRANSITION MODULE	• Rear Transition Module (RTM) Available for Access to I/O Interfaces through Industry Standard Connectors, Eliminating Need for Custom Harnessing or Complex Cabling Fixtures • I/O Support for an SFP+ CX4 Copper/Fiber interface port, 4x external SATA (eSATA) ports, two USB ports, 2x Gigabit Ethernet ports, RS-232/485 console port, and VGA port
OPTIONS	• Conformal Coating • Custom RTM • CPU-111-10 Integrated into VPX Chassis

3.2 Processing Architecture

3.2.1 Processor

The CPU-111-10 supports a 2.13GHz 4-Core Xeon L5408 Processor with 32KB data and 32KB of instruction cache per core and 12MB of L2 shared cache. Processor features include:

- One Intel quad-core L5408 Xeon Processor running at 2.13 GHz
- 32KB L1 Instruction and 32KB L1 Data Cache per core
- 12MB L2 Cache (shared)
- 1066/1333 MHz Front Side Bus supporting 8.5 GByte/Sec transfer rates

3.2.2 Memory Controller Hub and DDR2 SDRAM

The Intel® 5100 Memory Controller Hub (MCH) provides dual memory controllers and 24 lanes of PCI Express expansion (all of which are implemented on the CPU-111-10) for high-speed connectivity to dual XMC sites (8 lanes each) and a PLX PEX8624PCIe Switch (8 lanes) for further PCI Express distribution. The MCH supports up to 4 GBytes of DDR2 SDRAM running at up to 1066 MHz double data rate speeds. MCH features include:

- Intel 5100 MCH with 1066/1333 MHz Front Side Bus
- 4GB DDR2 ECC SDRAM at 533/667 MHz (1066 MHz DDR)
- Two x8 PCI Express Ports to XMC Sites
- One x8 PCI Express Port to PEX8624 Gen 2 PCIe Switch
- ESI Bus to ICH9R I/O Controller Hub

3.2.3 I/O Controller Hub

The Intel® ICH9R I/O Controller Hub (ICH) chipset provides basic I/O, and standard PC system resources including graphics, the real time clock, NV-RAM, timers, thermal management, and interrupt management. Features include:

- Four Serial ATA Ports to VPX P4 Connector
- Four USB Ports to VPX P4 Connector
- LPC Bus to 16Mbit Firmware Hub
- 16Mbit SPI Flash
- RS232/RS485 Serial Communications to VPX P4 Connector
- x1 PCIe Interface supports SM750 VGA Controller
- Real-time clock with 256 bytes of battery-backed RAM

3.3 PCI Express Architecture

The PCI Express (PCIe) structure is shown below. All PCIe links operate at Gen1 speeds. The CPU-111-10 does not support XMC based root complexes, only end-points.

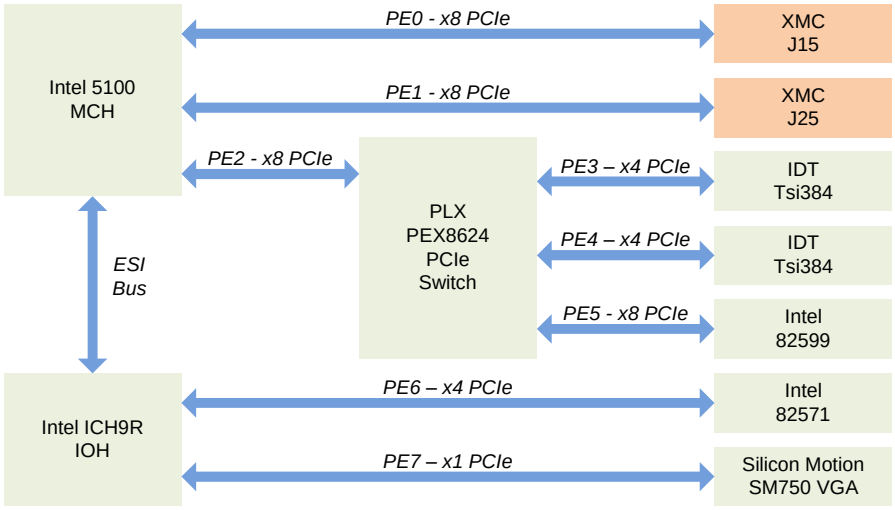


Figure 2: PCI Express Structure

The MCH provides 24 lanes of Gen1 PCIe and acts as the root complex. This is divided into three x8 ports. Two x8 ports connect to the XMC sites. The third x8 port connects to a PLX PEX8624 24-port Switch. This switch "fans out" the MCH PCIe further as two x4 PCIe links to two IDT Tsi384 PCIe to PCI-X Bridges, providing a PCI-X interface for each PMC site. The switch also supports a x8 link to an Intel 82599 Dual 10Gb Ethernet Controller, providing a high-speed connection in the on-board 10GB Ethernet switch fabric.

The ICH9R has two PCIe ports. One x4 port is connected to an Intel 82571 Dual 1Gb Ethernet Controller to support 1000BASE-T backplane control plane I/O. The remaining x1 PCIe port connects to a Silicon Motion SM750 Graphics Controller.

3.3.1 Dual XMC Sites

Each XMC Site can support a x8 Gen1 PCIe endpoint per VITA42.3 using connectors J15 and J25. XMC based root complexes are not supported on the CPU-111-10.

3.3.2 PLX PEX8624 PCIe Switch

The PEX8624 is a 6-port, 24-lane PCI Express switch configured as four ports. It has integrated low power SerDes on all lanes and supports a fully non-blocking switch architecture. Its cut-thru packet latency is less than 160nSec between symmetric ports (x8 and x8). The maximum data payload size is 2048 bytes.

3.3.2 IDT Tsi384 PCIe to PCI-X Bridges for PMC Support

The IDT Tsi384 is a high-performance bus bridge that efficiently connects the x4 PCIe link from the PEX8624 to a 64-bit 133MHz PCI-X bus. One Tsi384 is used per PMC site to maximize PCI-X transfer rates. The Tsi384's only support 3.3V PCI-X I/O signaling.

3.3.3 Intel 82599 Dual 10Gb Ethernet Controller

The Intel 82599 10 Gigabit Ethernet Controller is a single component with two fully integrated 10Gbit Ethernet MAC and XAUI ports. Each port can support KX4/KX (802.3ap*) interfaces and contains a SerDes for backward compatibility with gigabit backplanes. The architecture is designed for low-latency data handling and provides superior DMA transfer-rate performance. The 82599 also supports the IEEE 1588 precision time protocol (PTP) by time stamping in-coming and out-going data packets.

3.3.4 Intel 82571 Dual 1Gb Ethernet Controller

The Intel 82571 Gigabit Ethernet Controller is a single component containing two fully integrated Gigabit Ethernet Media Access Controllers and physical layer ports. Both ports contain a SerDes to support Gigabit backplane applications. The 82571 provides high performance and low memory latency using a x4 PCI Express link to the ICH9R I/O Hub.

- Complies with 1Gb/Sec Ethernet/802.3ap
- x4 PCI Express interface to ICH9R
- MDII or SERDES interface to backplane
- 4-Wire SPI EEPROM Interface

3.3.5 Silicon Motion SM750 Graphics Controller

The SM750 is a PCI Express 2D multimedia mobile display controller device, packaged in a 265-pin BGA. Designed to complement needs for the embedded industry, it provides video and 2D capability. It supports a wide variety of I/O, including an analog RGB, two Zoom Video interfaces, and Pulse Width Modulation (PWM).

The 2D engine includes a front-end color space conversion with 4:1 and 1:8 scaling support. The video engine supports two different video outputs (Dual Monitor), at 8-bit, 16-bit, or 32-bit per pixel and a 3-color hardware cursor per video output.

- Connects to ICH9R via x1 PCI Express Interface
- 16MByte Internal DDR SDRAM Video Memory
- 2D Graphics Accelerator
- DMA Controller

3.4 10 Gigabit Ethernet Architecture

The CPU-111-10 utilizes 10Gb Ethernet (10GbE) to provide high-speed interconnection paths between the CPU, both XMC sites, the backplane, and a front panel SFP+ module. The 10GbE architecture is shown below.

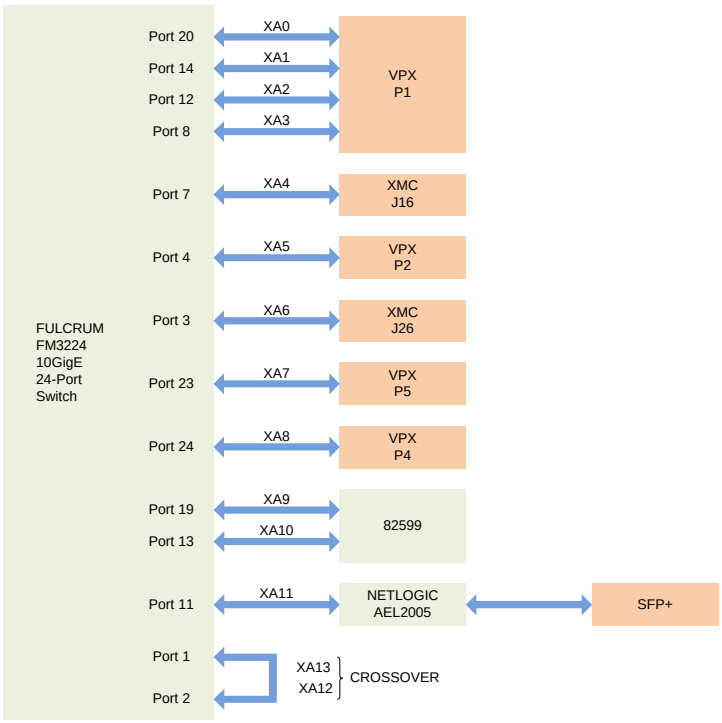


Figure 3: 10Gb Ethernet Architecture

3.4.1 Fulcrum FM3224 Switch

The FM3224 10GbE Switch is the heart of the CPU-111-10 SBC. Using 10Gb Ethernet, it connects the backplane to the CPU, XMC Modules, and front panel SFP+ Fiber Optic I/O modules (not included with the CPU-111-10).

The FM3224 is a fully integrated single-chip wire-speed 10G Ethernet switch. In addition to enhanced layer-2 functionality, the FM3224 layer-3 capabilities include advanced classification, extensive congestion management, and improved switch management flexibility.

Features of the FM3224 include:

- 300nS Latency
- Advanced Policy Engine
- Switch Virtualization and Scaling
- Port and MAC Based Security
- In-band Switch Management
- Provides Full-Mesh connectivity between up to eight VPQ Node Boards
- Support for Front Panel SFP+ Connector for Copper or Fiber Optic cables (Configuration dependent)

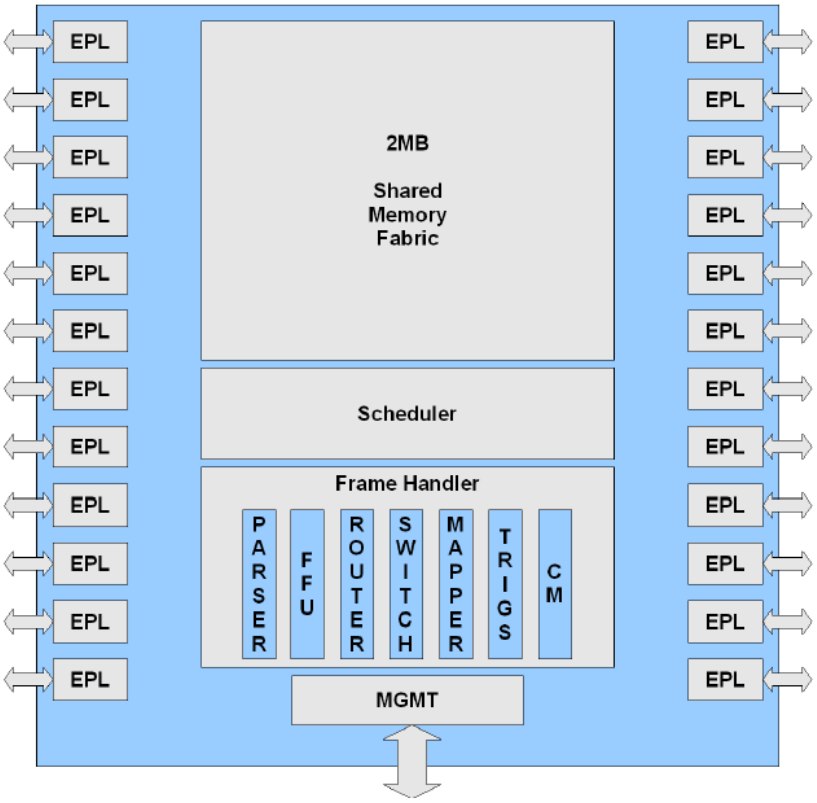


Figure 4: 10Gb Switch Block Diagram

3.4.2 Intel 82599 Dual 10GB Ethernet

The 82599 provides a high-speed CPU path into the switch fabric for both data and switch management . The interface to the switch consists of dual-channel XAUI (IEEE 802.3ae). The 82599 connects via x8 Gen2 PCIe to the PEX8624 PCIe switch and from there to the CPU. As previously mentioned, the 82599 also supports IEEE 1588 precision time protocol (PTP) by time stamping in-coming and out-going data packets.

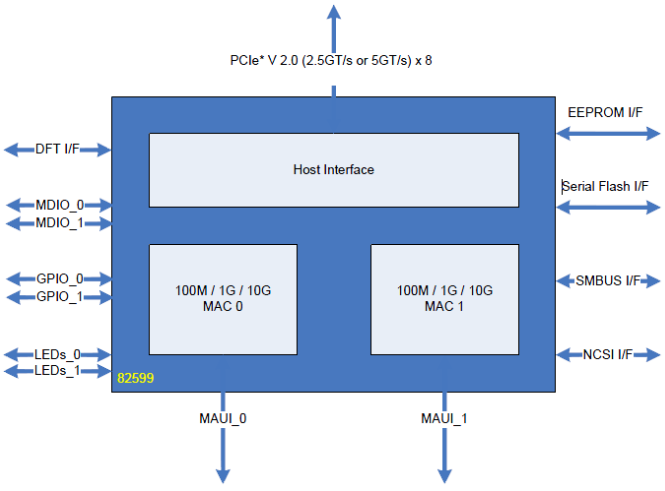


Figure 5: 82599 Block Diagram

3.4.3 SFP+ Interface (AEL2009)

The AEL2005 is a bidirectional single-channel 10 Gigabit Ethernet transceiver containing integrated EDC (Electronic Dispersion Compensation) circuits targeted for 10GBASE-LRM optical modules and 10Gbps SFP+ applications. The SFP+ connector is located on the CPU-111-10 front panel.

3.4.4 VPX 10Gb Ethernet I/O

Seven ports from the FM3224 10GbE switch are connected to the VPX backplane. The CPU-111-10 complies with the VITA 46 OpenVPX standard for profile MOD6-PAY-4F2T-12.2.2-5. This profile covers the four 10GbE channels on VPX connector P1. The remaining three 10GbE channels connect to P2, P4, and P5.

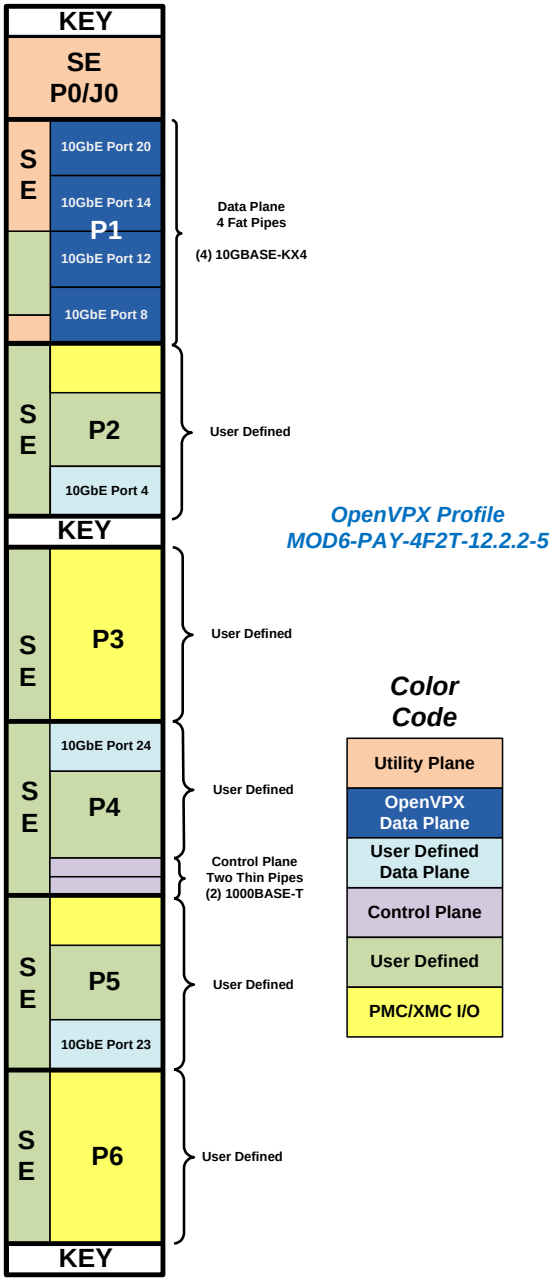


Figure 6: VPX 10GbE I/O

3.4.5 XMC 10GbE I/O

Each XMC site supports one 10GbE channel to provide a high-speed data path into the 10GbE switch fabric.

3.5 VPX General Purpose I/O

The CPU-111-10 provides general purpose I/O via VPX connector P4. This I/O can be connected to a rear transition module or can be terminated on the backplane. The I/O consists of (4) SATA ports, (4) USB ports, (1) LPC bus, (1) RS232/RS485 Serial Communications Port, (2) 1GbE SERDES channels, and (2) 1000BASE-T 1GbE ports.

3.6 Clocking

An IDT ICS9LPR501 CK505 Clock Synthesizer generates the majority of clocks used on the CPU-111-10. It generates 100MHz differential clocks used by the CPU and PCIe peripherals. It also generates 48MHz, 33MHz, and 14MHz clocks used throughout the CPU-111-10. Clocks for DDR SDRAM are generated by the MCH. Separate 312.5MHz and 125MHz oscillators provide clocks to the FM3224 10GbE Switch.

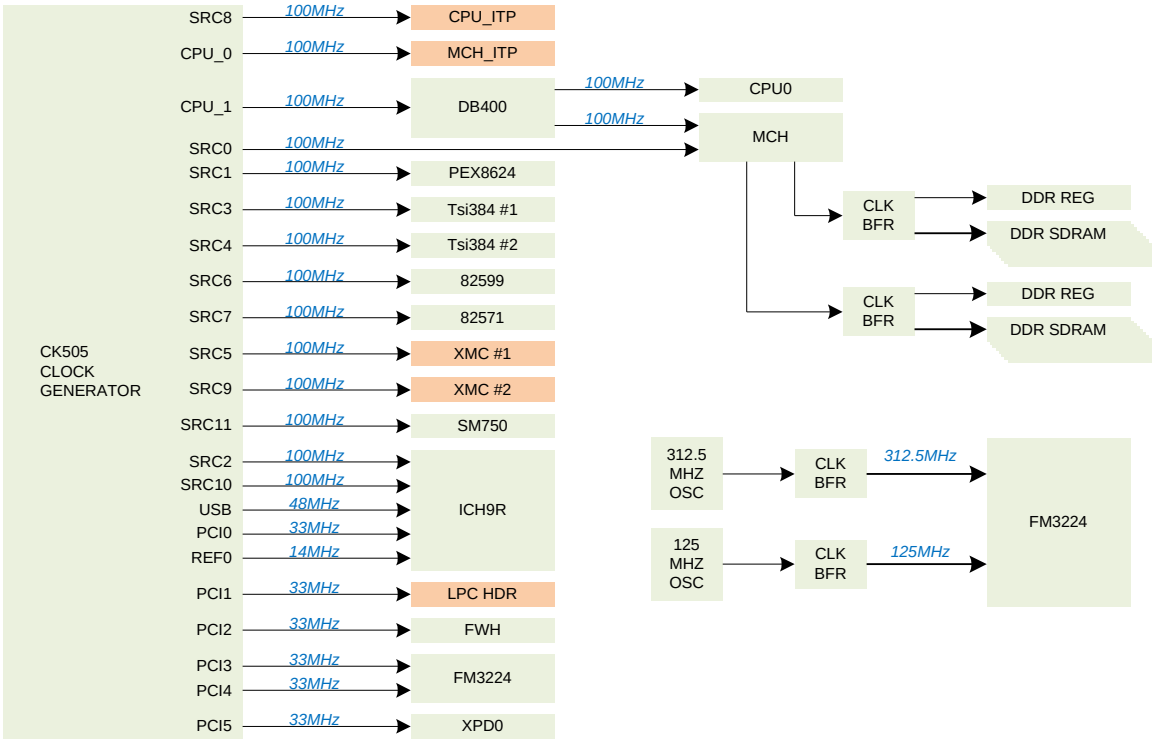


Figure 7: Clocks

3.7 Reset Structure

A block diagram of the CPU-111-10 reset structure is shown below. The ispPOWR1220A provides reset glue logic for the board. The backplane system reset (BP_SYSRST#) is an input when the CPU-111-10 is installed in a peripheral slot and an output when installed in the system controller slot.

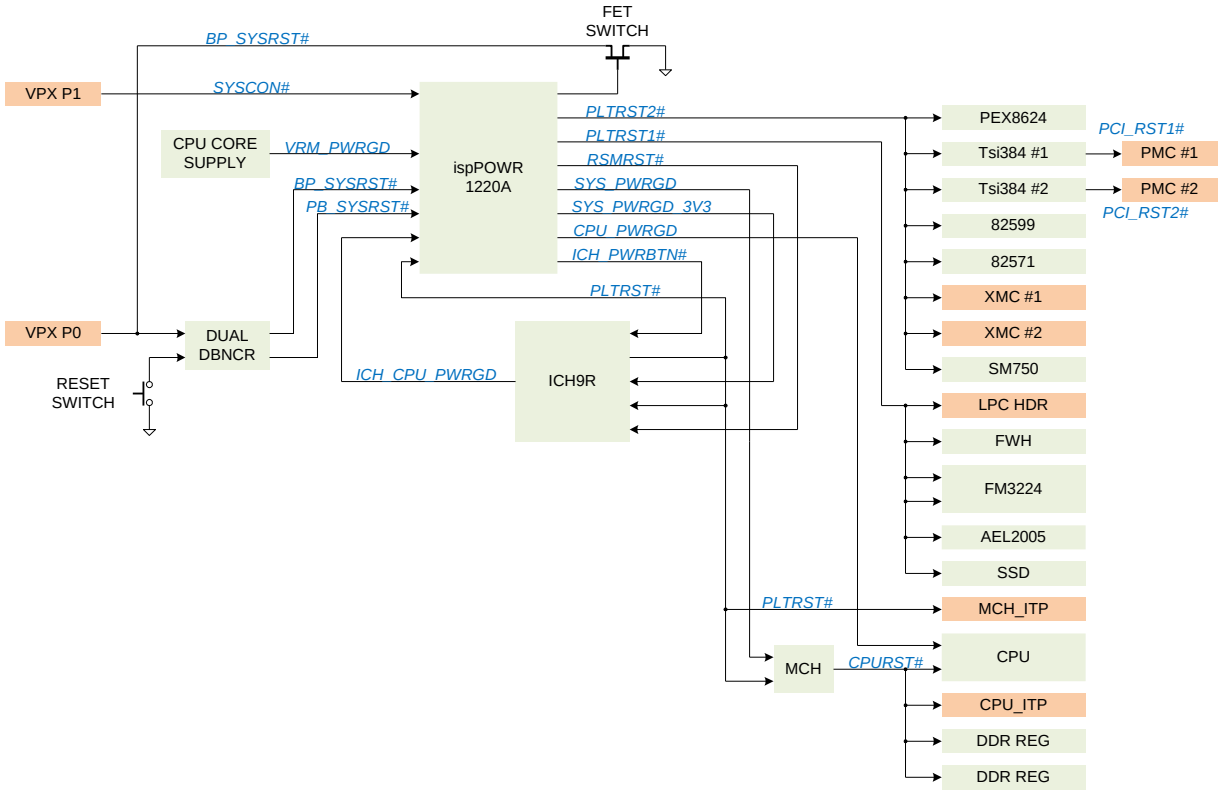


Figure 8: Reset Structure

When all non-core supplies are up and stable, the ICH9R release the platform reset, or PLTRST#. The 1220A buffers this reset and distributes it throughout the board as PLTRST1# and PLTRST2#. When PLTRST# is released and the CPU core supply is stable, the CPU reset is released and the board boots up.

3.8 SMBus Architecture

The CPU-111-10 utilizes an SMBus to support inter-chip communications. This can range from management functionality, e.g. reading temperature sensors, to setting up application specific operational conditions in the various peripheral components. The SMBus runs at a maximum speed of 100KHz.

The ICH9R SMBus connects to the MCH and an I2C Bus Multiplexer, where the bus is then distributed around the board. A separate SMBus connects the ICH9R to the FM3224 10GbE Switch to support initialization and out-of-band switch management.

SMB_A is connected to the CK505 Clock Generator, the DB400 Clock Buffer, the ispPOWR1220A power monitor/sequencer, various Temperature monitoring devices, and an I2C bus expander.

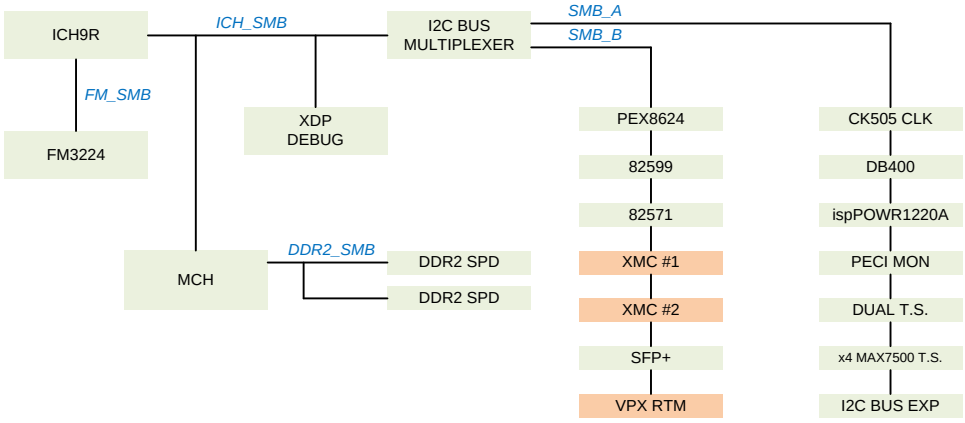


Figure 9: SMBus Architecture

The I2C bus expander provides GPIO for reading the board geographic address, system controller status, and the VPX backplane non-volatile memory read-only (NVMRO) status.

SMB_B is connected to the PEX8624 PCIe switch, the 82599 Dual 10GbE controller, 82571 dual 1GbE controller, both XMC sites, the front panel SFP+ connector, and to a rear transition module via the VPX backplane.

The MCH provides one SMBus port which connects to two serial presence detect (SPD) EEPROM's containing memory initialization parameters.

3.9 Board Power

There are 11 major supply rails on the CPU-111-10. A block diagram of the power supply architecture is shown below. The VPX backplane provides +12V and +5V supplies. The majority of the on-board supply rails are generated by Linear Technology LTM4616 16A MicroModules. A discrete DC-DC converter controlled by an Intersil ISL6314 provides the CPU core supply. Two switching FET's control backend 3.3 and 5V power. -12V is generated by an LTC3693 1A regulator and is only used by the dual PMC sites. Power monitoring and sequencing is performed by a programmable Lattice ispPOWR1220A.

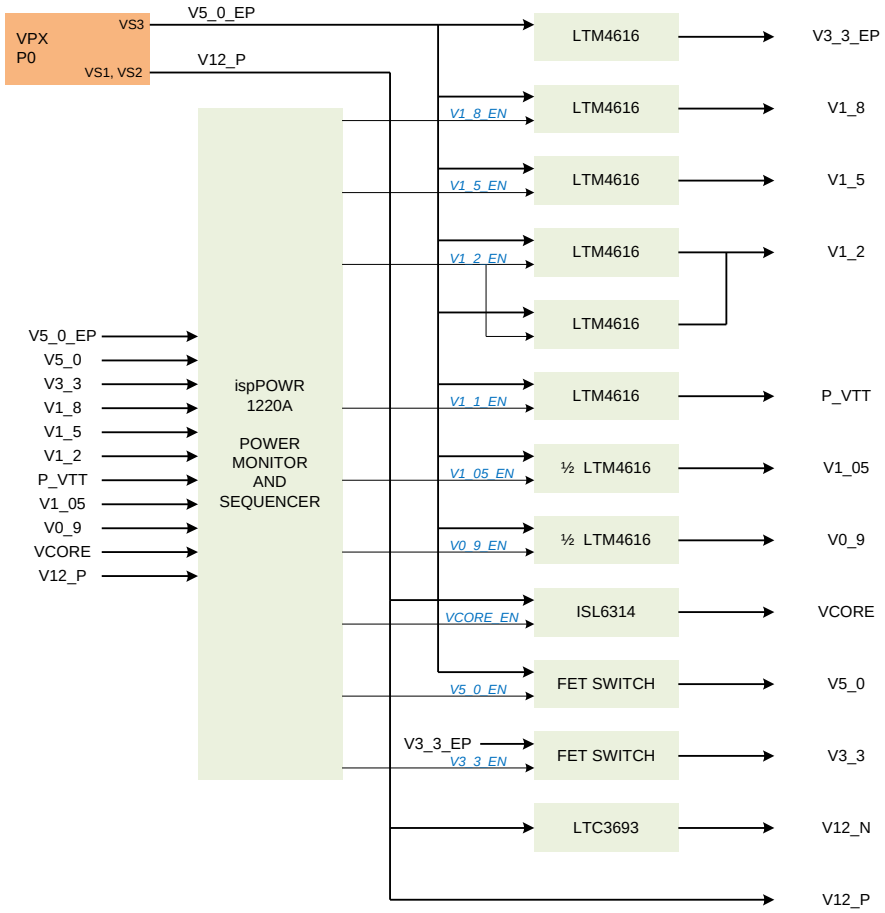


Figure 10: Power Generation & Distribution

For input power requirements please refer to Appendix C.

3.10 Rear Transition Module

The CPU-111-10 Rear Transition Module (RTM) provides I/O support for the CPU-111-10 SBC. This "Module Specific I/O" capability of the CPU-111-10 provides rear chassis I/O for a SFP+ CX4 Copper/Fiber interface port, Four External SATA (eSATA) ports, Two USB ports, dual 1Gb Ethernet ports, a RS232/485 Console port, and a VGA port.

Four 2mm headers are provided to support CPU-111-10 PMC Module I/O. J1 and J3 terminate the signals derived from PMC J14 and J2 and J4 terminate signals from J24. Please refer to Appendix D for RTM pin assignments.

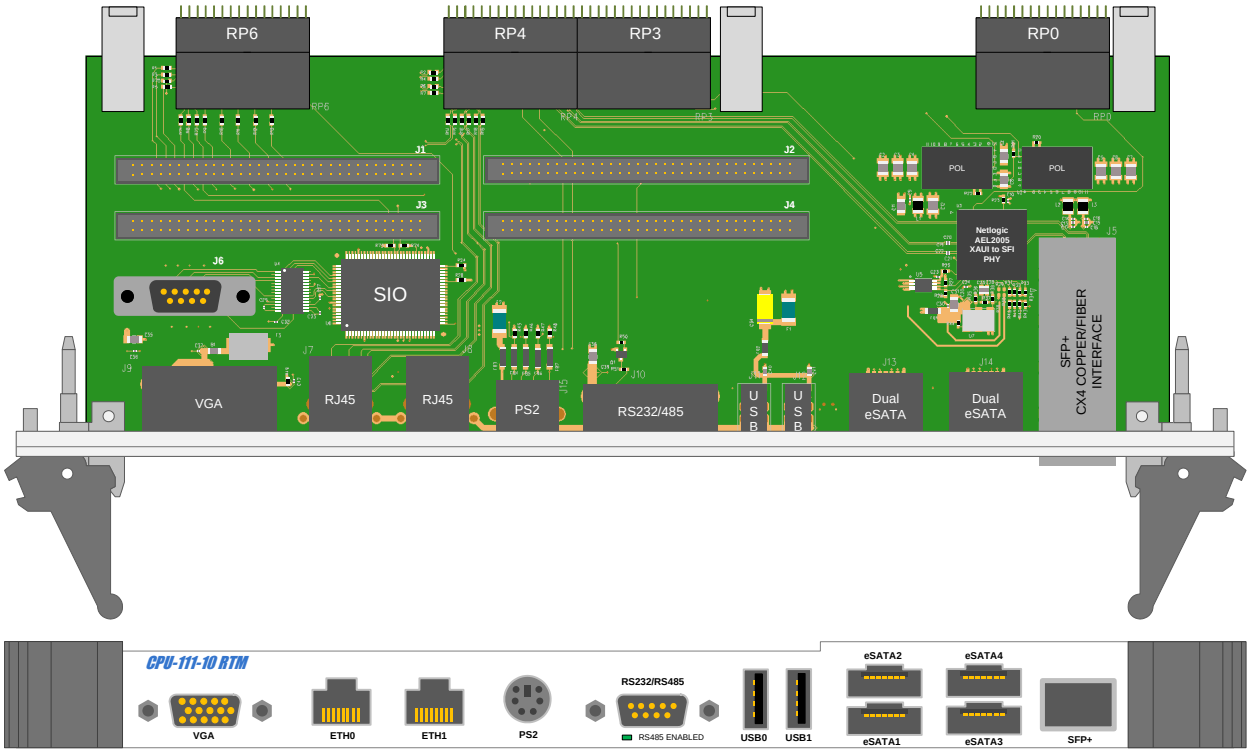


Figure 11: Rear Transition Module

4. Installation

*** UNDER CONSTRUCTION ***

The following sections cover the steps necessary to configure the CPU-111-10 and install it into a 6U VPX system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

4.1 Selectable Options

This section explains how to set up user configurable jumpers.

The CPU-111-10 is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

The CPU-111-10 contains x jumpers...

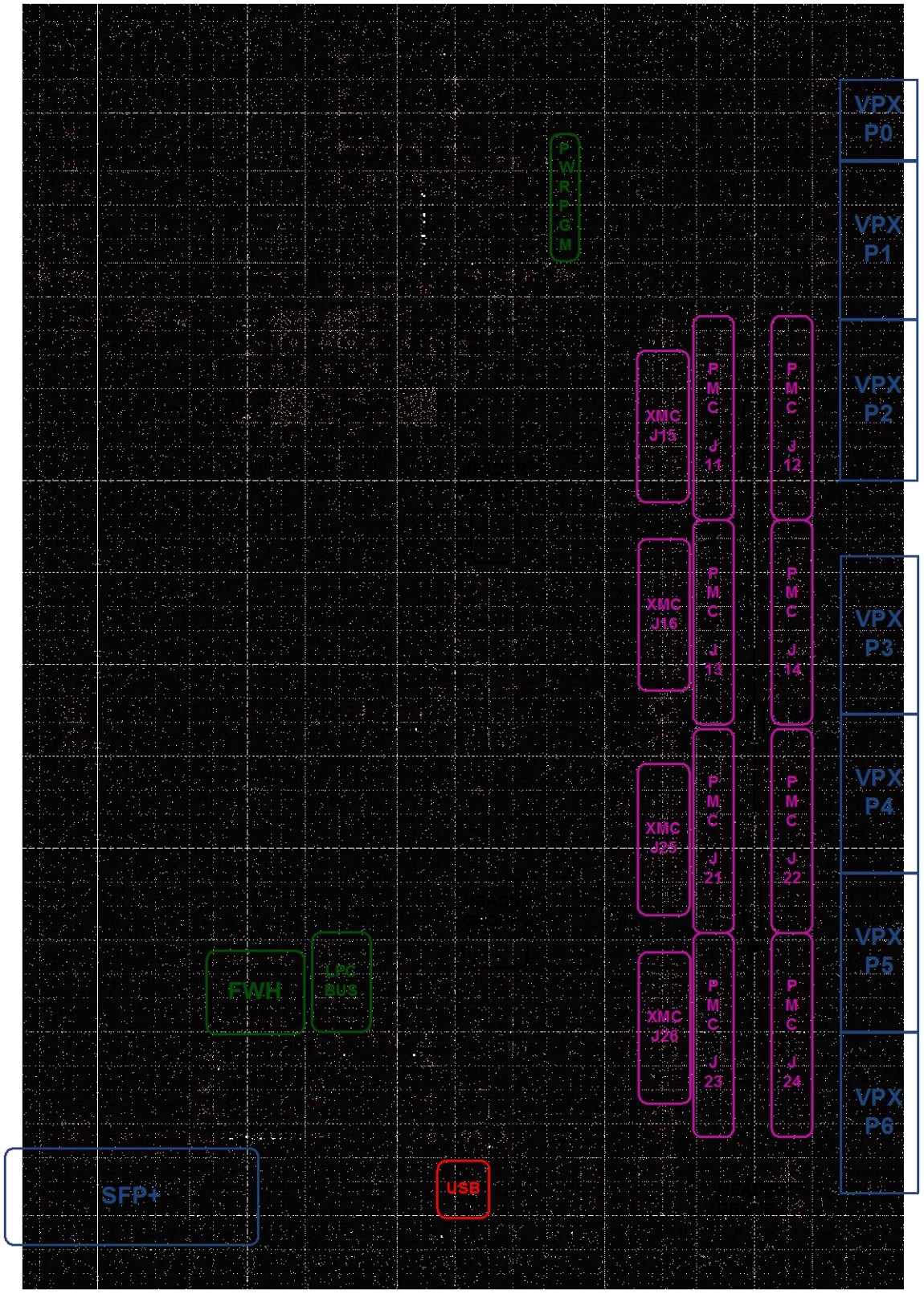


Figure 12: CPU-111-10 Connectors and Headers

4.2 PCI Mezzanine Card (PMC) Installation

4.3 Front Panel Connectors and Reset Switch

The CPU-111-10 supports two PMC/XMC sites, an SFP+ connector, and an optional USB port. Front panel indicators consist of a green power on LED, a red CPU Error LED, a yellow System Controller LED, and a yellow solid state drive activity LED. A small hole is provided for access to recessed reset switch.

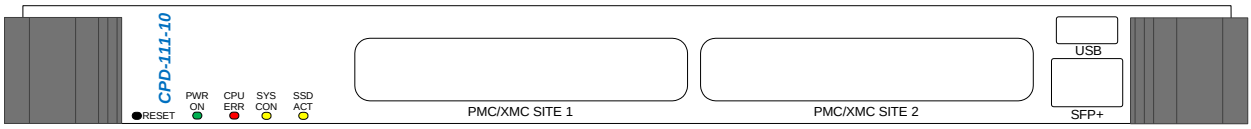


Figure 13: Front Panel Connectors and Indicators

A. Connector Pin-outs

A.1 VPX Backplane Connectors

Table 1: VPX P0 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Power	Vs1 (12V)	Vs1 (12V)	Vs1 (12V)	No Pad	Vs2 (12V)	Vs2 (12V)	Vs2 (12V)	
2	Power	Vs1 (12V)	Vs1 (12V)	Vs1 (12V)	No Pad	Vs2 (12V)	Vs2 (12V)	Vs2 (12V)	
3	Power	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)	No Pad	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)	
4	Single-ended			GND		GND	SYSRESET#	NVMRO	
5	Single-ended	GAP#	GA4#	GND		GND			***VITA 46.0***
6	Single-ended	GA3#	GA2#	GND		GND	GA1#	GA0#	
7	Differential		GND			GND			
8	Differential	GND			GND			GND	

Table 2: VPX P1 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Differential		GND	XAUI0_TX0-	XAUI0_TX0+	GND	XAUI0_RX0-	XAUI0_RX0+	Data Plane 1 (Fat Pipe)
2	Differential	GND	XAUI0_TX1-	XAUI0_TX1+	GND	XAUI0_RX1-	XAUI0_RX1+	GND	
3	Differential		GND	XAUI0_TX2-	XAUI0_TX2+	GND	XAUI0_RX2-	XAUI0_RX2+	**10GBASE-BX4**
4	Differential	GND	XAUI0_TX3-	XAUI0_TX3+	GND	XAUI0_RX3-	XAUI0_RX3+	GND	
5	Differential	SYS_CON#	GND	XAUI1_TX0-	XAUI1_TX0+	GND	XAUI1_RX0-	XAUI1_RX0+	Data Plane 2 (Fat Pipe)
6	Differential	GND	XAIU1_TX1-	XAIU1_TX1+	GND	XAIU1_RX1-	XAIU1_RX1+	GND	
7	Differential		GND	XAIU1_TX2-	XAIU1_TX2+	GND	XAIU1_RX2-	XAIU1_RX2+	**10GBASE-BX4**
8	Differential	GND	XAIU1_TX3-	XAIU1_TX3+	GND	XAIU1_RX3-	XAIU1_RX3+	GND	
9	Differential		GND	XAIU2_TX0-	XAIU2_TX0+	GND	XAIU2_RX0-	XAIU2_RX0+	Data Plane 3 (Fat Pipe)
10	Differential	GND	XAIU2_TX1-	XAIU2_TX1+	GND	XAIU2_RX1-	XAIU2_RX1+	GND	
11	Differential		GND	XAIU2_TX2-	XAIU2_TX2+	GND	XAIU2_RX2-	XAIU2_RX2+	**10GBASE-BX4**
12	Differential	GND	XAIU2_TX3-	XAIU2_TX3+	GND	XAIU2_RX3-	XAIU2_RX3+	GND	
13	Differential		GND	XAIU3_TX0-	XAIU3_TX0+	GND	XAIU3_RX0-	XAIU3_RX0+	Data Plane 4 (Fat Pipe)
14	Differential	GND	XAIU3_TX1-	XAIU3_TX1+	GND	XAIU3_RX1-	XAIU3_RX1+	GND	
15	Differential		GND	XAIU3_TX2-	XAIU3_TX2+	GND	XAIU3_RX2-	XAIU3_RX2+	**10GBASE-BX4**
16	Differential	GND	XAIU3_TX3-	XAIU3_TX3+	GND	XAIU3_RX3-	XAIU3_RX3+	GND	
							VITA 46.7 r0.05		***OpenVPX MOD6-PAY-4F2T-12.2.2-4***

Table 3: VPX P2 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Differential		GND	J16-A5 (DP04+)	J16-B5 (DP04-)	GND	J16-D5 (DP05+)	J16-E5 (DP05-)	
2	Differential	GND	J16-A7 (DP06+)	J16-B7 (DP06-)	GND	J16-D7 (DP07+)	J16-E7 (DP07-)	GND	
3	Differential		GND	J16-A9 (DP08+)	J16-B9 (DP08-)	GND	J16-D9 (DP09+)	J16-E9 (DP09-)	***VITA 46.9 r0.23 XMC Site 1 X12d Pattern Map***
4	Differential	GND	J16-A15 (DP14+)	J16-B15 (DP14-)	GND	J16-D15 (DP15+)	J16-E15 (DP15-5)	GND	
5	Differential		GND	J16-A17 (DP16+)	J16-B17 (DP16-)	GND	J16-D17 (DP17+)	J16-E17 (DP17-)	
6	Differential	GND	J16-A19 (DP18+)	J16-B19 (DP18-)	GND	J16-D19 (DP19+)	J16-E19 (DP19-)	GND	
7	Differential		GND			GND			
8	Differential	GND			GND			GND	
9	Differential		GND			GND			
10	Differential	GND			GND			GND	
11	Differential		GND			GND			
12	Differential	GND			GND			GND	
13	Differential		GND	XAIU5_TX0-	XAIU5_TX0+	GND	XAIU5_RX0-	XAIU5_RX0+	User Defined Data Plane 5 (Fat Pipe)
14	Differential	GND	XAIU5_TX1-	XAIU5_TX1+	GND	XAIU5_RX1-	XAIU5_RX1+	GND	
15	Differential		GND	XAIU5_TX2-	XAIU5_TX2+	GND	XAIU5_RX2-	XAIU5_RX2+	**10GBASE-BX4**
16	Differential	GND	XAIU5_TX3-	XAIU5_TX3+	GND	XAIU5_RX3-	XAIU5_RX3+	GND	

Table 4: VPX P3 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Differential	RTM_MDIO	GND	J14-1	J14-3	GND	J14-2	J14-4	
2	Differential	GND	J14-5	J14-7	GND	J14-6	J14-8	GND	
3	Differential	RTM_MDC	GND	J14-9	J14-11	GND	J14-10	J14-12	
4	Differential	GND	J14-13	J14-15	GND	J14-14	J14-16	GND	
5	Differential	RTM_PWREN	GND	J14-17	J14-19	GND	J14-18	J14-20	
6	Differential	GND	J14-21	J14-23	GND	J14-22	J14-24	GND	
7	Differential	RTM_PWRGD	GND	J14-25	J14-27	GND	J14-26	J14-28	***PMC Site 1***
8	Differential	GND	J14-29	J14-31	GND	J14-30	J14-32	GND	
9	Differential	RTM_PBRST#	GND	J14-33	J14-35	GND	J14-34	J14-36	***VITA 46.9 r0.23 P64s Pattern Map***
10	Differential	GND	J14-37	J14-39	GND	J14-38	J14-40	GND	
11	Differential	SMB_B_DAT	GND	J14-41	J14-43	GND	J14-42	J14-44	
12	Differential	GND	J14-45	J14-47	GND	J14-46	J14-48	GND	
13	Differential	SMB_B_CLK	GND	J14-49	J14-51	GND	J14-50	J14-52	
14	Differential	GND	J14-53	J14-55	GND	J14-54	J14-56	GND	
15	Differential	RS485_EN	GND	J14-57	J14-59	GND	J14-58	J14-60	
16	Differential	GND	J14-61	J14-63	GND	J14-62	J14-64	GND	

Table 5: VPX P4 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Differential		GND	XAUI8_TX0-	XAUI8_TX0+	GND	XAUI8_RX0-	XAUI8_RX0+	User Defined Data Plane 6 (Fat Pipe)
2	Differential	GND	XAUI8_TX1-	XAUI8_TX1+	GND	XAUI8_RX1-	XAUI8_RX1+	GND	
3	Differential	VGA_SDA	GND	XAUI8_TX2-	XAUI8_TX2+	GND	XAUI8_RX2-	XAUI8_RX2+	**10GBASE-BX4**
4	Differential	GND	XAUI8_TX3-	XAUI8_TX3+	GND	XAUI8_RX3-	XAUI8_RX3+	GND	
5	Differential	VGA_SCL	GND	SATA1_TX-	SATA1_TX+	GND	SATA1_RX-	SATA1_RX+	User Defined
6	Differential	GND	SATA2_TX-	SATA2_TX+	GND	SATA2_RX-	SATA2_RX+	GND	
7	Differential	VGA_HS	GND	SATA3_TX-	SATA3_TX+	GND	SATA3_RX-	SATA3_RX+	**(4) Serial ATA**
8	Differential	GND	SATA4_TX-	SATA4_TX+	GND	SATA4_RX-	SATA4_RX+	GND	
9	Differential	VGA_VS	GND	USB0-	USB0+	GND	USB1-	USB1+	User Defined
10	Differential	GND	RS232_TX or RS485_TX-	RS232_RTS or RS485_TX+	GND	RS232_CTS or RS485_RX-	RS232_RX or RS485_RX+	GND	**(2) USB, Serial Comm**
11	Differential	VGA_R	GND	SERDES0_TX-	SERDES0_TX+	GND	SERDES0_RX-	SERDES0_RX+	User Defined
12	Differential	GND	SERDES1_TX-	SERDES1_TX+	GND	SERDES1_RX-	SERDES1_RX+	GND	**(2) Ultra Thin-Pipes**
13	Differential	VGA_B	GND	MDXB_1-	MDXB_1+	GND	MDXB_0-	MDXB_0+	Control Plane 1 (Thin Pipe) **1000 BASE-T**
14	Differential	GND	MDXB_3-	MDXB_3+	GND	MDXB_2-	MDXB_2+	GND	
15	Differential	VGA_G	GND	MDXA_1-	MDXA_1+	GND	MDXA_0-	MDXA_0+	Control Plane 2 (Thin Pipe) **1000 BASE-T**
16	Differential	GND	MDXA_3-	MDXA_3+	GND	MDXA_2-	MDXA_2+	GND	

OpenVPX
MOD6-PAY-4F2T-12.2.2-4

Table 6: VPX P5 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1	Differential		GND	J26-A5 (DP04+)	J26-B5 (DP04-)	GND	J26-D5 (DP05+)	J26-E5 (DP05-)	***XMC Site 2***
2	Differential	GND	J26-A7 (DP06+)	J26-B7 (DP06-)	GND	J26-D7 (DP07+)	J26-E7 (DP07-)	GND	
3	Differential		GND	J26-A9 (DP08+)	J26-B9 (DP08-)	GND	J26-D9 (DP09+)	J26-E9 (DP09-)	***VITA 46.9 r0.23***
4	Differential	GND	J26-A15 (DP14+)	J26-B15 (DP14-)	GND	J26-D15 (DP15+)	J26-E15 (DP15-)	GND	***X12d Pattern Map***
5	Differential		GND	J26-A17 (DP16+)	J26-B17 (DP16-)	GND	J26-D17 (DP17+)	J26-E17 (DP17-)	
6	Differential	GND	J26-A19 (DP18+)	J26-B19 (DP18-)	GND	J26-D19 (DP19+)	J26-E19 (DP19-)	GND	
7	Differential		GND			GND			
8	Differential	GND			GND			GND	
9	Differential		GND			GND			
10	Differential	GND			GND			GND	
11	Differential		GND			GND			
12	Differential	GND			GND			GND	
13	Differential		GND	XAIU7_TX0-	XAIU7_TX0+	GND	XAIU7_RX0-	XAIU7_RX0+	User Defined Data Plane 7 (Fat Pipe)
14	Differential	GND	XAIU7_TX1-	XAIU7_TX1+	GND	XAIU7_RX1-	XAIU7_RX1+	GND	
15	Differential		GND	XAIU7_TX2-	XAIU7_TX2+	GND	XAIU7_RX2-	XAIU7_RX2+	**10GBASE-BX4**
16	Differential	GND	XAIU7_TX3-	XAIU7_TX3+	GND	XAIU7_RX3-	XAIU7_RX3+	GND	

Table 7: VPX P6 Connector Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Differential	EEP_WP	GND	J24-1	J24-3	GND	J24-2	J24-4
2	Differential	GND	J24-5	J24-7	GND	J24-6	J24-8	GND
3	Differential		GND	J24-9	J24-11	GND	J24-10	J24-12
4	Differential	GND	J24-13	J24-15	GND	J24-14	J24-16	GND
5	Differential		GND	J24-17	J24-19	GND	J24-18	J24-20
6	Differential	GND	J24-21	J24-23	GND	J24-22	J24-24	GND
7	Differential		GND	J24-25	J24-27	GND	J24-26	J24-28
8	Differential	GND	J24-29	J24-31	GND	J24-30	J24-32	GND
9	Differential		GND	J24-33	J24-35	GND	J24-34	J24-36
10	Differential	GND	J24-37	J24-39	GND	J24-38	J24-40	GND
11	Differential		GND	J24-41	J24-43	GND	J24-42	J24-44
12	Differential	GND	J24-45	J24-47	GND	J24-46	J24-48	GND
13	Differential		GND	J24-49	J24-51	GND	J24-50	J24-52
14	Differential	GND	J24-53	J24-55	GND	J24-54	J24-56	GND
15	Differential		GND	J24-57	J24-59	GND	J24-58	J24-60
16	Differential	GND	J24-61	J24-63	GND	J24-62	J24-64	GND

PMC Site 2

VITA 46.9 r0.23
P64s Pattern Map

A.2 PCI-X Mezzanine Card Connectors

Table 8: PCI-X Mezzanine Card Connector Pin-outs

J11, J12, J21, J22 PMC CONNECTORS

Pin	J11/J21		Pin	Pin	J12/J22		Pin
1		V12_N	2	1	V12_P		2
3	GND	INTA#	4	3			4
5	INTB#	INTC#	6	5		GND	6
7		V5_0	8	7	GND		8
9	INTD#		10	9			10
11	GND	V3_3_AUX	12	11		V3_3	12
13	CLK	GND	14	13	RESET#		14
15	GND	GNT#	16	15	V3_3		16
17	REQ#	V5_0	18	17	PME#	GND	18
19	VIO	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	GND	AD[26]	22
23	AD[25]	GND	24	23	AD[24]	V3_3	24
25	GND	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	V3_3	AD[20]	28
29	AD[19]	V5_0	30	29	AD[18]	GND	30
31	VIO	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	GND	34	33	GND		34
35	GND	IRDY#	36	35	TRDY#	V3_3	36
37	DEVSEL#	V5_0	38	37	GND	STOP#	38
39	GND	LOCK#	40	39	PERR#	GND	40
41			42	41	V3_3	SERR#	42
43	PAR	GND	44	43	C/BE[1]#	GND	44
45	VIO	AD[15]	46	45	AD[14]	AD[13]	46
47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[9]	V5_0	50	49	AD[8]	V3_3	50
51	GND	C/BE[0]#	52	51	AD[7]		52
53	AD[6]	AD[5]	54	53	V3_3		54
55	AD[4]	GND	56	55		GND	56
57	VIO	AD[3]	58	57			58
59	AD[2]	AD[1]	60	59	GND		60
61	AD[0]	V5_0	62	61	ACK64#	V3_3	62
63	GND	REQ64#	64	63	GND		64

J13, J14, J23, J24 PMC CONNECTORS

Pin	J13/J23		Pin
1		GND	2
3	GND	C/BE[7]#	4
5	C/BE[6]#	C/BE[5]#	6
7	C/BE[4]#	GND	8
9	VIO	PAR64	10
11	AD[63]	AD[62]	12
13	AD[61]	GND	14
15	GND	AD[60]	16
17	AD[59]	AD[58]	18
19	AD[57]	GND	20
21	VIO	AD[56]	22
23	AD[55]	AD[54]	24
25	AD[53]	GND	26
27	GND	AD[52]	28
29	AD[51]	AD[50]	30
31	AD[49]	GND	32
33	GND	AD[48]	34
35	AD[47]	AD[46]	36
37	AD[45]	GND	38
39	VIO	AD[44]	40
41	AD[43]	AD[42]	42
43	AD[41]	GND	44
45	GND	AD[40]	46
47	AD[39]	AD[38]	48
49	AD[37]	GND	50
51	GND	AD[36]	52
53	AD[35]	AD[34]	54
55	AD[33]	GND	56
57	VIO	AD[32]	58
59			60
61		GND	62
63	GND		64

Pin	J14 *(x=1) / J24 (x=2)*		Pin
1	Px4_1	Px4_2	2
3	Px4_3	Px4_4	4
5	Px4_5	Px4_6	6
7	Px4_7	Px4_8	8
9	Px4_9	Px4_10	10
11	Px4_11	Px4_12	12
13	Px4_13	Px4_14	14
15	Px4_15	Px4_16	16
17	Px4_17	Px4_18	18
19	Px4_19	Px4_20	20
21	Px4_21	Px4_22	22
23	Px4_23	Px4_24	24
25	Px4_25	Px4_26	26
27	Px4_27	Px4_28	28
29	Px4_29	Px4_30	30
31	Px4_31	Px4_32	32
33	Px4_33	Px4_34	34
35	Px4_35	Px4_36	36
37	Px4_37	Px4_38	38
39	Px4_39	Px4_40	40
41	Px4_41	Px4_42	42
43	Px4_43	Px4_44	44
45	Px4_45	Px4_46	46
47	Px4_47	Px4_48	48
49	Px4_49	Px4_50	50
51	Px4_51	Px4_52	52
53	Px4_53	Px4_54	54
55	Px4_55	Px4_56	56
57	Px4_57	Px4_58	58
59	Px4_59	Px4_60	60
61	Px4_61	Px4_62	62
63	Px4_63	Px4_64	64

A.3 XMC connectors

Table 9: XMC Connector Pin-outs

J15 – Primary Site 1 XMC Connector per VITA 42.3

	Row F	Row E	Row D	Row C	Row B	Row A	
1	VPWR	PE0_TX1n	PE0_TX1p	V3_3	PE0_TX0n	PE0_TX0p	1
2	RESET#	GND	GND		GND	GND	2
3	VPWR	PE0_TX3n	PE0_TX3p	V3_3	PE0_TX2n	PE0_TX2p	3
4		GND	GND		GND	GND	4
5	VPWR	PE0_TX5n	PE0_TX5p	V3_3	PE0_TX4n	PE0_TX4p	5
6	V12_P	GND	GND		GND	GND	6
7	VPWR	PE0_TX7n	PE0_TX7p	V3_3	PE0_TX6n	PE0_TX6p	7
8	V12_N	GND	GND		GND	GND	8
9	VPWR						9
10	GA0 ('b0)	GND	GND		GND	GND	10
11	VPWR	PE0_RX1n	PE0_RX1p		PE0_RX0n	PE0_RX0p	11
12		GND	GND	GA1 ('b0)	GND	GND	12
13	VPWR	PE0_RX3n	PE0_RX3p	V3_3	PE0_RX2n	PE0_RX2p	13
14	SMB_B_DAT	GND	GND	GA2 ('b0)	GND	GND	14
15	VPWR	PE0_RX5n	PE0_RX5p		PE0_RX4n	PE0_RX4p	15
16	SMB_B_CLK	GND	GND	NVMRO	GND	GND	16
17		PE0_RX7n	PE0_RX7p		PE0_RX6n	PE0_RX6p	17
18		GND	GND		GND	GND	18
19			WAKE#		REFCLKn	REFCLKp	19

J16 – Secondary Site 1 XMC Connector

	Row F	Row E	Row D	Row C	Row B	Row A	
1		XA4_TX1n	XA4_TX1p		XA4_TX0n	XA4_TX0p	1
2		GND	GND		GND	GND	2
3		XA4_TX3n	XA4_TX3p		XA4_TX2n	XA4_TX2p	3
4		GND	GND		GND	GND	4
5		P16_DP05n	P16_DP05p		P16_DP04n	P16_DP04p	5
6		GND	GND		GND	GND	6
7		P16_DP07n	P16_DP07p		P16_DP06n	P16_DP06p	7
8		GND	GND		GND	GND	8
9		P16_DP09n	P16_DP09p		P16_DP08n	P16_DP08p	9
10		GND	GND		GND	GND	10
11		XA4_RX1n	XA4_RX1p		XA4_RX0n	XA4_RX0p	11
12		GND	GND		GND	GND	12
13		XA4_RX3n	XA4_RX3p		XA4_RX2n	XA4_RX2p	13
14		GND	GND		GND	GND	14
15		P16_DP15n	P16_DP15p		P16_DP14n	P16_DP14p	15
16		GND	GND		GND	GND	16
17		P16_DP17n	P16_DP17p		P16_DP16n	P16_DP16p	17
18		GND	GND		GND	GND	18
19		P16_DP19n	P16_DP19p		P16_DP18n	P16_DP18p	19

J25 – Primary Site 2 XMC Connector per VITA 42.3

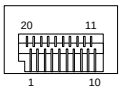
	Row F	Row E	Row D	Row C	Row B	Row A	
1	VPWR	PE1_TX1n	PE1_TX1p	V3_3	PE1_TX0n	PE1_TX0p	1
2	RESET#	GND	GND		GND	GND	2
3	VPWR	PE1_TX3n	PE1_TX3p	V3_3	PE1_TX2n	PE1_TX2p	3
4		GND	GND		GND	GND	4
5	VPWR	PE1_TX5n	PE1_TX5p	V3_3	PE1_TX4n	PE1_TX4p	5
6	V12_P	GND	GND		GND	GND	6
7	VPWR	PE1_TX7n	PE1_TX7p	V3_3	PE1_TX6n	PE1_TX6p	7
8	V12_N	GND	GND		GND	GND	8
9	VPWR						9
10	GA0 ('b1)	GND	GND		GND	GND	10
11	VPWR	PE1_RX1n	PE1_RX1p		PE1_RX0n	PE1_RX0p	11
12		GND	GND	GA1 ('b0)	GND	GND	12
13	VPWR	PE1_RX3n	PE1_RX3p	V3_3	PE1_RX2n	PE1_RX2p	13
14	SMB_B_DAT	GND	GND	GA2 ('b0)	GND	GND	14
15	VPWR	PE1_RX5n	PE1_RX5p		PE1_RX4n	PE1_RX4p	15
16	SMB_B_CLK	GND	GND	NVMRO	GND	GND	16
17		PE1_RX7n	PE1_RX7p		PE1_RX6n	PE1_RX6p	17
18		GND	GND		GND	GND	18
19			WAKE#		REFCLKn	REFCLKp	19

J26 – Secondary Site 2 XMC Connector

	Row F	Row E	Row D	Row C	Row B	Row A	
1		XA6_TX1n	XA6_TX1p		XA6_TX0n	XA6_TX0p	1
2		GND	GND		GND	GND	2
3		XA6_TX3n	XA6_TX3p		XA6_TX2n	XA6_TX2p	3
4		GND	GND		GND	GND	4
5		P26_DP05n	P26_DP05p		P26_DP04n	P26_DP04p	5
6		GND	GND		GND	GND	6
7		P26_DP07n	P26_DP07p		P26_DP06n	P26_DP06p	7
8		GND	GND		GND	GND	8
9		P26_DP09n	P26_DP09p		P26_DP08n	P26_DP08p	9
10		GND	GND		GND	GND	10
11		XA6_RX1n	XA6_RX1p		XA6_RX0n	XA6_RX0p	11
12		GND	GND		GND	GND	12
13		XA6_RX3n	XA6_RX3p		XA6_RX2n	XA6_RX2p	13
14		GND	GND		GND	GND	14
15		P26_DP15n	P26_DP15p		P26_DP14n	P26_DP14p	15
16		GND	GND		GND	GND	16
17		P26_DP17n	P26_DP17p		P26_DP16n	P26_DP16p	17
18		GND	GND		GND	GND	18
19		P26_DP19n	P26_DP19p		P26_DP18n	P26_DP18p	19

A.4 SFP+ Pin-out

Table 10: SFP+ Connector Pin-outs

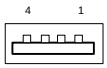


SFP+ Connector

Pin	Signal	Pin	Signal
1	GND	11	GND
2	TX_FAULT	12	RD-
3	TX_DISABLE	13	RD+
4	SDA	14	GND
5	SCL	15	3.3V
6	MOD_DETECT	16	3.3V
7		17	GND
8	RX_LOS	18	TD+
9		19	TD-
10	GND	20	GND

A.5 Front Panel USB Pin-out

Table 11: USB Connector Pin-out

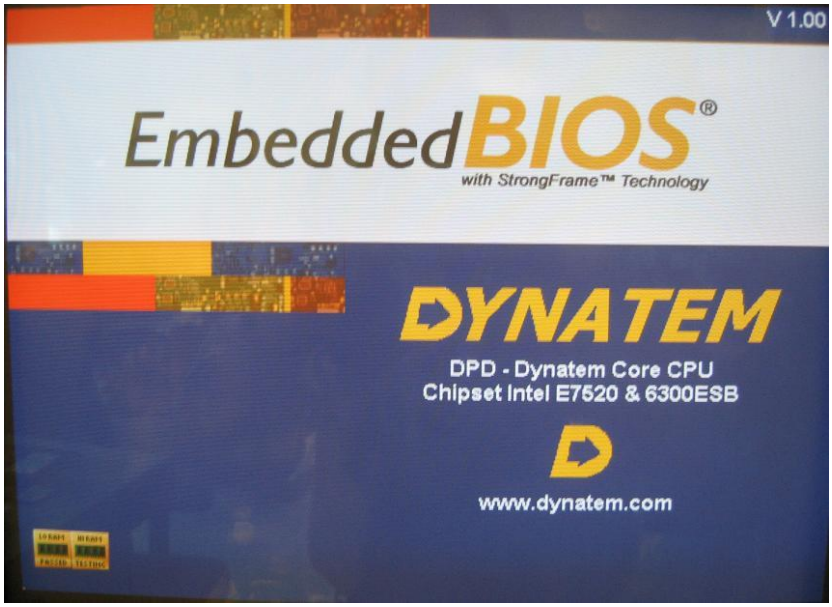


USB Connectors

Pin	Signal
1	5V
2	USB-
3	USB+
4	GND

B. BIOS & Setup *** NEED INPUT FROM HUNG ***

The CPU-111-10 uses General Software's Embedded BIOS with StrongFrame™ Technology, Rev 6.The BIOS is configured with the System Setup Utility, accessible from the Preboot Menu. This photo shows the initial splash screen that is displayed after powering up the system as the BIOS runs through the Power On Self Test (POST). When your system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components.



To enter the Setup mode, please press the delete <Del> key on your keyboard after powering up your system, during POST.

B.1 Redirecting to a Serial Port

Setup may be run from the main keyboard and video display or from a terminal emulator program running on a host computer connected to the system through a serial cable. To use a serial port, connect a dumb terminal or a PC running a terminal emulation utility like Hyperterminal to COM1 via a null modem. Next, set the communications parameters of the host's terminal program to 115Kbaud. Other parameters are 8-bit, no parity, and one stop bit. Do not enable XON/XOFF or hardware flow control.

With this link set up, power on the system. Press ^C a few times on your dumb terminal or your PC as the system boots. POST will redirect to the serial console, and after it has completed its early stages, it will start the preboot menu.

B.2 Setup Menus

The standard Embedded BIOS setup menus are described below in the order they generally appear in the menuing system (Dynatem cannot vouch for support for all BIOS functions described in the subsequent sections):

Main	Display main system components and allow editing of date and time.
Exit	Save changes and exit, discard changes and exit, or restore factory default settings.
Boot	Configure boot actions and boot devices.
POST	Configure POST.
PnP	Configure Plug-n-Play for non-ACPI OSes.
SIO	Configure Super I/O devices such as serial ports and parallel ports.
Features	Enable and disable system BIOS features like ACPI, APM, PnP, MP, quick boot, and the splash screen.
Firmbase	Configure Firmbase Technology and the features that use it, such as USB keyboard and mouse support (commonly, USB HID), boot from USB (commonly, USB Boot), and applications such as high availability, boot security (not user security, but chain-of-trust security), and network-based remote access.
Misc	Configure miscellaneous BIOS settings that do not fall into any other category.
Shadowing	Configure chipset shadow RAM regions.
Security	Configure which BIOS features require user authentication before they perform their functions
CUI	Configure the layout and coloring of the Common User Interface (CUI) display engine that supports preboot applications.
Chipset	Configure any chipset-specific parameters, such as memory, CPU, and bus timing, and availability of chipset-specific features such as TFT support. Highly platform-specific and entirely up to the OEM's implementation.

B.3 Navigating Setup Menus and Fields

Navigation (moving your cursor around, selecting items, and changing them) is easy in theSetup system. The following chart is a helpful user reference:

UP key (also ^E)	Move the cursor to the line above, scrolling the window as necessary.
DOWN key (also ^X)	Move the cursor to the line below, scrolling the window as necessary.
LEFT key	Go back to the menu to the left of the currently-displayed menu in the menu bar.
RIGHT key	Go forward to the menu to the right of the currently-displayed menu in the menu bar.
PGUP key	Move the cursor up several lines (a full window's worth), scrolling the window as necessary.
PGDN key	Move the cursor down several lines (a full window's worth), scrolling the window as necessary.
HOME key	Move the cursor to the first configurable field in the current menu, scrolling the window as necessary.
END key	Move the cursor to the last configurable field in the current menu, scrolling the window as necessary.
ESC key	Exit the Setup system, discarding all changes(except date/time changes, which take place on-the-fly.)
TAB key	Move the cursor down to the next configurable field.
Shift-TAB key (backtab)	Move the cursor up to the last configurable field.
+ key	Toggle an Enable/Disable field, or increase a numeric field's value.
- key	Toggle an Enable/Disable field, or decrease a numeric field's value.
SPACE key	Toggle an Enable/Disable field.

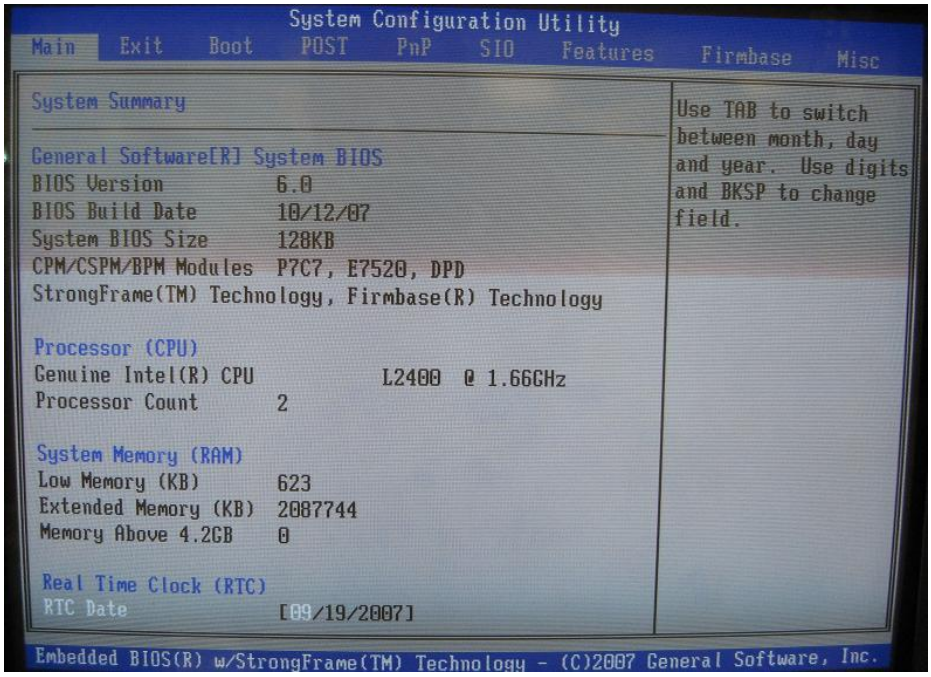
BKSP key	Reset an Enable/Disable or multiple-choice field, or back-up in numeric or string fields.
Digits (0-9)	Used to enter numeric parameters.
Alphabetic (A-Z, a-z)	Used to enter text data on ASCII fields such as email addresses.
Special symbols (!@#$%^&*_-+={}[], etc.)	Used to enter special text on ASCII fields that permit these characters.

The basic idea when using the Setup system is to navigate to the menus containing fields you want to review, and change those fields as desired. When your settings are complete, navigate to the EXIT menu, and select "Save Settings and Restart". This causes the settings to be stored in nonvolatile memory in the system, and the system will reboot so that POST can configure itself with the new settings.

After rebooting it may be desirable to reenter the Setup system as necessary to adjust settings as necessary. Once the system boots, the Setup system cannot be entered; this is because the memory used by the BIOS configuration manager is deallocated by the system BIOS, so that it can be used by the OS when it boots. To reenter the Setup system after boot, simply reset the system or power off and power back on.

B.4 Main Setup Menu

The first menu always showing in the Setup system is the Main menu (unless disabled by the OEM.) This menu is shown in Figure 3.1 below.


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
System Summary
General Software[R] System BIOS
BIOS Version 6.0
BIOS Build Date 10/12/07
System BIOS Size 128KB
CPM/CSPM/BPM Modules P7C7, E7520, DPD
StrongFrame(TM) Technology, Firmbase(R) Technology
Processor (CPU)
Genuine Intel(R) CPU L2400 @ 1.66GHz
Processor Count 2
System Memory (RAM)
Low Memory (KB) 623
Extended Memory (KB) 2087744
Memory Above 4.2GB 0
Real Time Clock (RTC)
RTC Date [09/19/2007]
Use TAB to switch between month, day and year. Use digits and BKSP to change field.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The Main menu provides a system summary about the BIOS, processor, system memory, date and time, and any other items configured by the OEM. The BIOS information is obtained by Setup from the internal system BIOS build itself; this information is useful when obtaining support for your system.

PLEASE CALL Dynatem at (800)543-2830 FOR BIOS SUPPORT; DO NOT CALL GENERAL SOFTWARE DIRECTLY.

BIOS Version	Indicates the major and minor core architecture versions (6.x, where x is a number from 0 to 999.)

BIOS Build Date	Date in MM/DD/YY format on which Dynatem built the system BIOS binary file.
System BIOS Size	Size of BIOS exposed in low memory below the 1MB boundary. Commonly, 128KB would mean that the BIOS is visible in the address space from E000:0000 to F000:FFFF.
CPM/CSPM/BPM Modules	Indicates the names of the key architectural modules used to create the system BIOS binary file. The CPM module provides the CPU family support; the CSPM module provides the northbridge support; and the BPM module provides the board-level support.

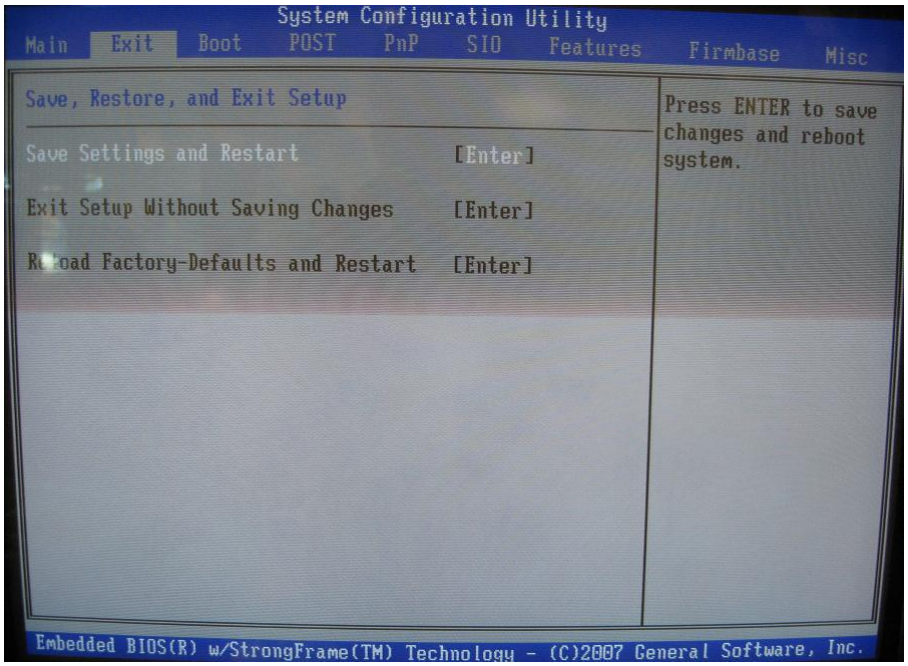
The CPU information is normally obtained by querying the Processor Brand String in the CPU's MSRs; the method used to achieve this is beyond the scope of this document.

The system memory information does not describe physical RAM; rather it describes the RAM as configured, subtracting RAM used for System Management Mode, Shadowing, Video buffers, and other uses. This provides realistic values about how much memory is actually available to operating systems and applications.

The Real Time Clock fields are editable with keystrokes. To navigate through the MM/DD/YYYY and HH:MM:SS fields, use the TAB and BACKTAB keys. The hours are normally specified in military time; thus 13 means 1pm, or one hour after noon, whereas 01 means 1am, or one hour after midnight. When the cursor leaves RTC fields, they either affect the battery-backed RTC right away, allowing the system to continue with your new settings, or they revert back to old values if the new values are not valid entries.

B.5 Exit Setup Menu

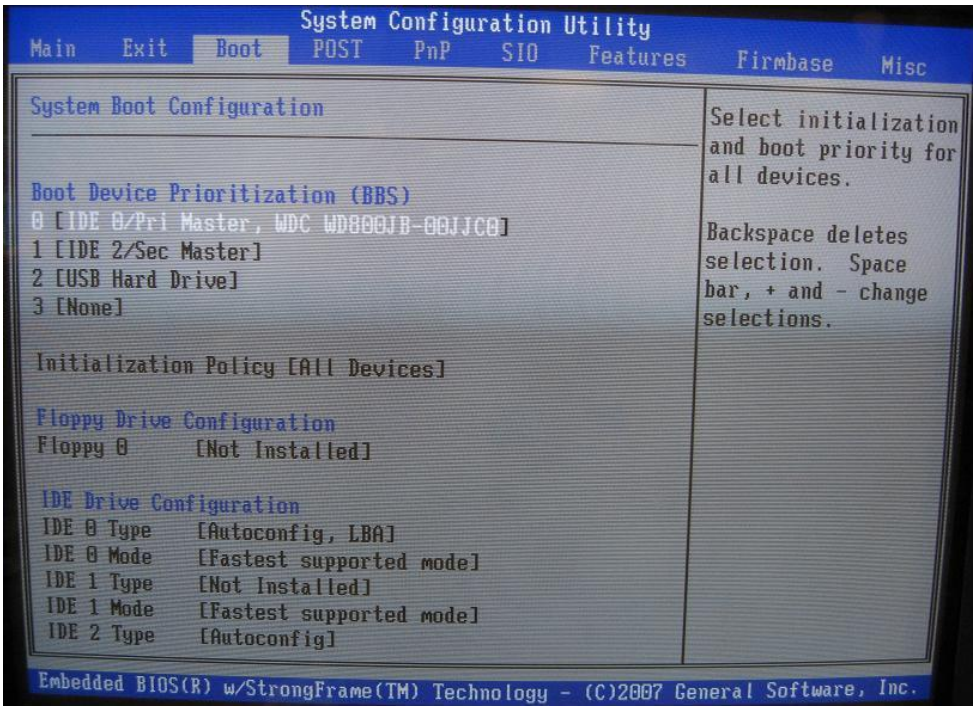
The Exit menu provides methods for saving changes made in other menus, discarding changes, or reloading the standard system settings. This menu is shown in Figure 3.2 below.



To select any of these options, position the cursor over the option and press the ENTER key. Pressing the ESC key at any time within the Setup system is equivalent to requesting "Exit Setup Without Saving Changes."

B.6 Boot Setup Menu

The Boot menu allows the system's boot actions and boot devices to be configured. This menu is shown here:


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
System Boot Configuration
Boot Device Prioritization (BBS)
0 [IDE 0/Pri Master, WDC WD800JB-00JJC0]
1 [IDE 2/Sec Master]
2 [USB Hard Drive]
3 [None]
Initialization Policy [All Devices]
Floppy Drive Configuration
Floppy 0 [Not Installed]
IDE Drive Configuration
IDE 0 Type [Autoconfig, LBA]
IDE 0 Mode [Fastest supported mode]
IDE 1 Type [Not Installed]
IDE 1 Mode [Fastest supported mode]
IDE 2 Type [Autoconfig]
Select initialization and boot priority for all devices.
Backspace deletes selection. Space bar, + and - change selections.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The BBS portion of this menu lists the devices and activities to be performed in the order in which they appear in the list. When the BIOS completes POST, it follows this list, attempting to process each item. Some items are drives, such as an ATA/IDE drive, or a USB hard disk, or CDROM.

The ordering of the drives in the BBS list controls the BIOS in several ways. First, it is the list of drives that is scanned and assigned BIOS unit numbers for DOS (for example 80h, 81h, 83h, and so on for hard drives). If a drive on the list is not plugged in or working properly, the BIOS moves on to the next drive, skipping the inoperative one.

Second, once the drives in the list have been verified, POST attempts to boot from them in that order as well. Drives without bootable partitions might be configured, but skipped over in the boot phase, so that other drives on the list become candidates for booting the OS.

The BBS list also contains other boot actions, such as boot from network cards and PCI slots, as well as special BIOS boot actions like "Boot EFI", "Boot Windows CE", or even "Boot Debugger". When deciding what boot action to do first and then next in succession, POST first scans all the drives in the list to verify they are present and operating properly (as described earlier in this section) and then goes down the list and tries to perform the actions in order. During this boot phase, if the list item is a drive, an attempt is made to boot from the boot record of that drive. If the list item is a device like a network card or PCI slot, an attempt is made to boot from that device. If the list item is a software item like "Boot Debugger", then it performs that action, and when that action completes, it moves on to the next item in the BBS list.

The table that follows lists the set of standard boot action items:

"drive name" – The system BIOS may list the drive's name in a generic sense (i.e., "USB Hard Drive") if the drive has not been detected yet, or the drive's full manufacturing name and serial number (if	Boot from the MBR/PBR of the named BIOSaware IPL drive (BAID). The drive may be Legacy Floppy, PATA, SATA, Compact Flash, or a USB drive.

detected.)	
IDE0/Primary Master Primary	Master PATA drive or SATA mapping by the chipset, routed to the backplane via J5.
IDE1/Primary Slave	Primary Slave PATA drive or SATA mapping by the chipset, routed to the backplane via J5.
IDE2/Secondary Master	Secondary Master PATA drive or SATA mapping by the chipset, routed to on-baord CompactFlash
IDE CDROM	First detected IDE CDROM.
USB Floppy Drive	First detected USB floppy drive.
USB Hard Drive	First detected USB hard drive.
USB CDROM Drive	First detected USB CDROM.
Enter Board Information Browser	Invoke HTML Browser on 0.HTM in ROM.
Enter BIOS Setup Screen	Invoke System Setup Utility in ROM.
Enter BIOS Debugger	Invoke BIOS debugger in ROM.
Reboot System	Restart system.
Power Off System	Invoke S5 state, powering off system.
PCI Slot [n]	Boot from device in PCI Slot 'n'.
Network	Boot from any network adapter.
SCSI	Boot from external SCSI device (on PMC/XMC card).
Boot EFI Binary	Boot EFI kernel from ROM or disk, depending on the EFI source setting in the Features menu. If disk is selected, then the BIOS searches all the configured disks in the system in the order they appear in the BBS list, attempting to load EFILDR.BIN from the root directory in the FAT file system located on those drives.
Boot Windows CE Image	Boot Windows CE kernel from disk. The BIOS searches all the configured disks in the system in the order they appear in the BBS list, attempting to load NK.BIN from the root directory in the FAT file system located on those drives.
Boot Graphical Desktop	Boot Firmbase GUI supporting graphical Firmbase applications as well as booting DOS in a graphical window. For applications requiring instant-on functionality even when the OS is not available or is still loading.

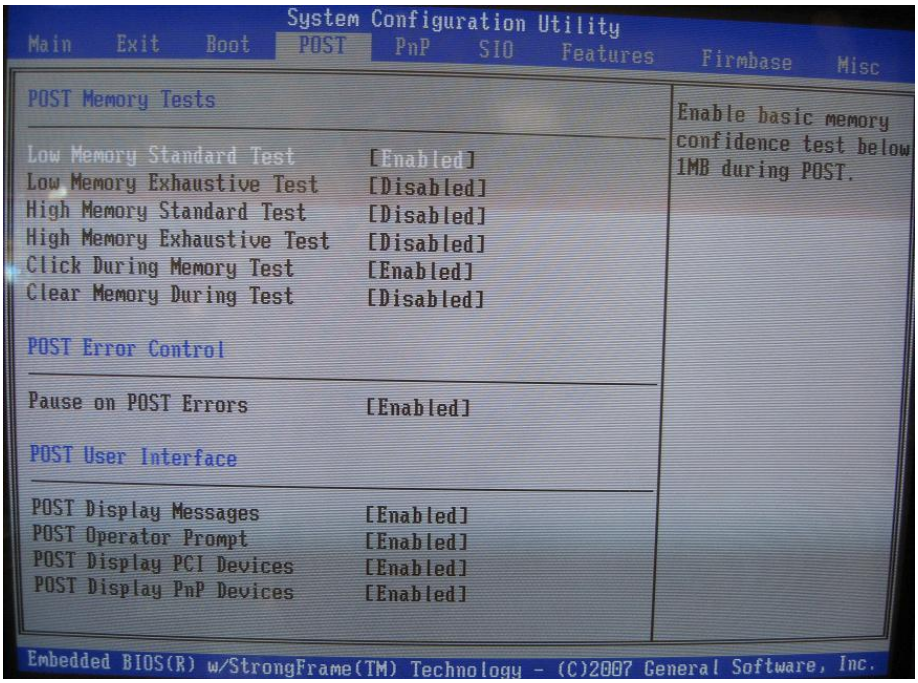
The photograph above shows a common setup of the BBS list for desktop applications. In this example, the first boot device is theWestern Digital IDE hard drive (WDC WD800JB-00JJC0) connected to the target as a Primary Master IDE drive. The second boot device is the Secondary Master and this is the on-board CompactFlash. The third device is a USB Hard Drive. A fourth boot device, "None", is a placeholder that is simply used to add more entries in the setup screen; "None" is not actually executed by POST as a boot action item.

In addition to the BBS boot device list, there are two more sections in the BOOT menu; namely, the Floppy Drive Configuration and IDE Drive Configuration sections. Both of these sections tell the BIOS what kind of equipment is connected to the motherboard but the floppy drive interface has not been implemented so please ignore this and leave it as "Not Installed". Similarly, the IDE Drive Configuration section describes the type of hard drive equipment that is connected to the motherboard, including the cable type. IDE drives, or actually more properly Parallel ATA (PATA) drives, are connected to the motherboard with a flat cable with either 40 or 80 wires running in parallel (hence, Parallel ATA, as opposed to Serial ATA.) The 40-pin connector supports speeds up to UDMA2, whereas 80-pin cables are needed for higher transfer rates to eliminate noise. The BIOS can be told what type of cable is available, so that it knows whether higher transfer rates are allowed; or, it can be told to autodetect the cable type, in which case the drive and the motherboard must both support the hardware protocol used to autodetect the drive's cable type.

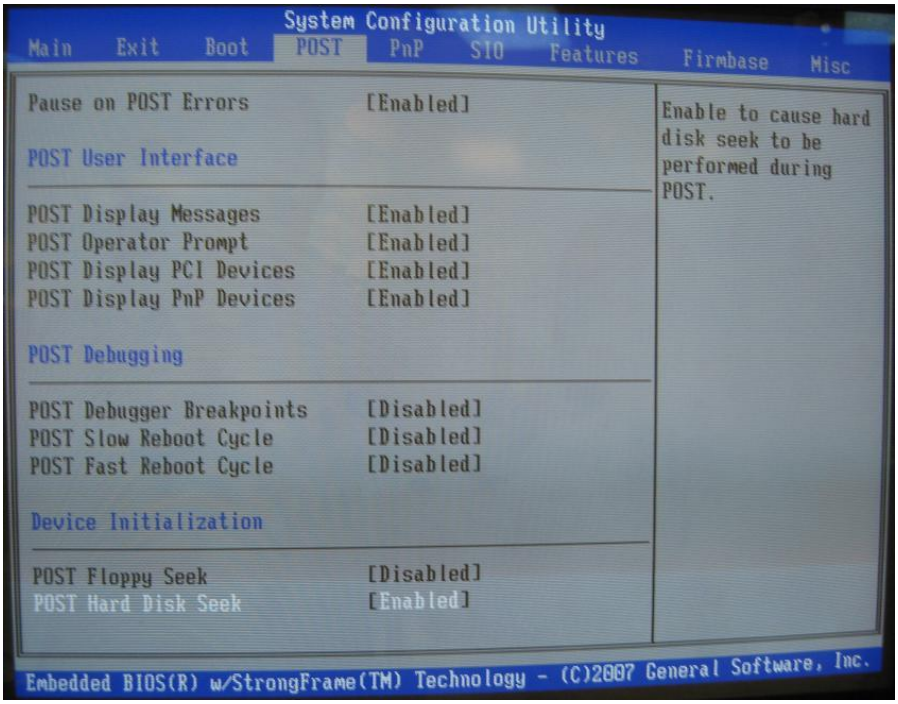
Note: PATA cable autodetection sometimes fails with older drives, so 40-pin is the default, to ensure data integrity. For higher performance, you should change this setting to 80-pin or AUTO if an 80-pin cable is installed.

B.7 POST Setup Menu

The POST menu is used to configure POST. This menu is shown in the following figure (scrolled down more so the full set of options can be seen.) Be sure to review the Features menu, where additional items can be configured, such as the Splash Screen and BIOS initiatives.


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
POST Memory Tests
Low Memory Standard Test [Enabled]
Low Memory Exhaustive Test [Disabled]
High Memory Standard Test [Disabled]
High Memory Exhaustive Test [Disabled]
Click During Memory Test [Enabled]
Clear Memory During Test [Disabled]
POST Error Control
Pause on POST Errors [Enabled]
POST User Interface
POST Display Messages [Enabled]
POST Operator Prompt [Enabled]
POST Display PCI Devices [Enabled]
POST Display PnP Devices [Enabled]
Enable basic memory confidence test below 1MB during POST.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The figure below shows the same menu, scrolled down so that the remainder of its fields may be viewed.


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
Pause on POST Errors [Enabled]
POST User Interface
POST Display Messages [Enabled]
POST Operator Prompt [Enabled]
POST Display PCI Devices [Enabled]
POST Display PnP Devices [Enabled]
POST Debugging
POST Debugger Breakpoints [Disabled]
POST Slow Reboot Cycle [Disabled]
POST Fast Reboot Cycle [Disabled]
Device Initialization
POST Floppy Seek [Disabled]
POST Hard Disk Seek [Enabled]
Enable to cause hard disk seek to be performed during POST.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The following table describes the settings associated with the POST setup menu's Memory Test section.

Low Memory Standard Test	Enable basic memory confidence test, of memory below 1MB address boundary (conventional memory, or memory normally used by DOS.)
Low Memory Exhaustive Test	Enable exhaustive memory confidence test of memory below 1MB address boundary.
High Memory Standard Test	Enable basic memory confidence test, of memory between 1MB and 4.2GB address boundaries (extended memory.)
High Memory Exhaustive Test	Enable exhaustive memory confidence test, of memory between 1MB and 4.2GB address boundaries.
Huge Memory Standard Test	Enable basic memory confidence test, of memory above 4.2GB address boundary (available using PAE technology.)
Huge Memory Exhaustive Test	Enable exhaustive memory confidence test, of memory above 4.2GB address boundary.
Click During Memory Test	Enable/disable speaker click when testing each block.
Clear Memory During Test	Enable storing 0's in all memory locations tested. Only necessary when some legacy DOS programs are run, as they may rely on cleared memory to operate properly.

The following table describes the settings associated with the POST setup menu's Error Control section:

Pause on POST Errors	Enable pause when errors are detected during POST, so that the user can view the error message and enter Setup or continue to boot the OS.

The following table describes the settings associated with the POST setup menu's POST User Interface section:

POST Display Messages	Enable display of text messages during POST. When disabled, POST is "quiet."
POST Operator Prompt	Enable operator prompts if POST is configured to ask interactive questions of the user about whether to load specific features; i.e., whether or not to load SMM.
POST Display PCI Devices	Enable display of PCI devices.
POST Display PnP Devices	Enable display of ISA PnP devices.

The following table describes the settings associated with the POST setup menu's Debugging section:

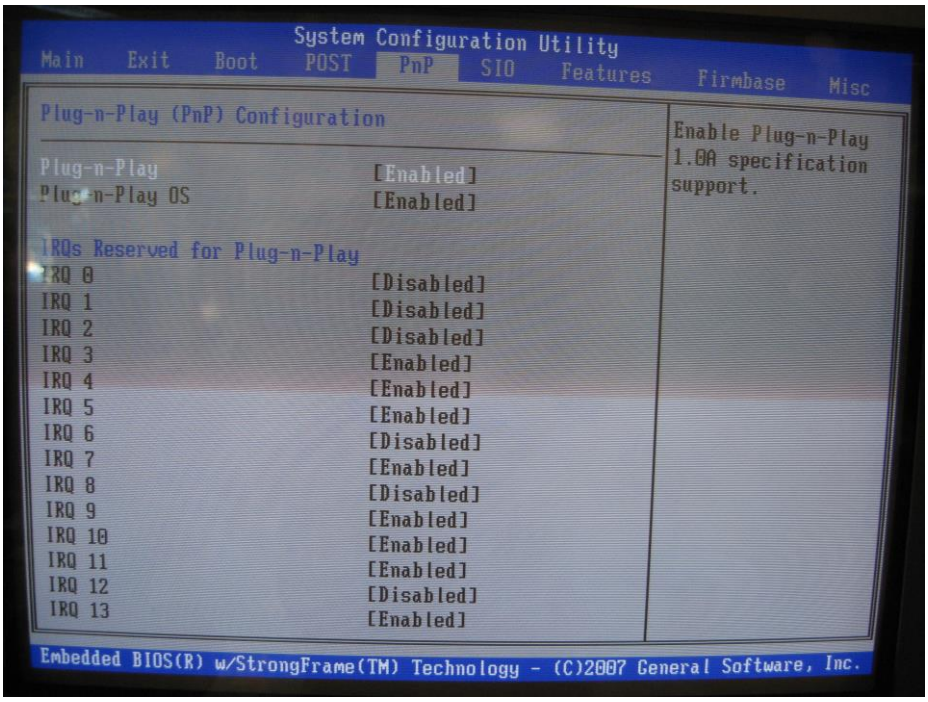
POST Debugger Breakpoints	Enable processing of INT 3 (breakpoint) instructions embedded into option ROMs. When enabled, if an INT 3 instruction is encountered, control is transferred to the BIOS debugger, so that the option ROM can be debugged. When disabled, these instructions perform no action.
POST Fast Reboot Cycle	Enable early reboot in POST, allowing service technician to verify that the hardware can technician to verify that the hardware can reboot very quickly many times in succession. Platform will continue to reboot after every boot until the system's CMOS is reset, as there is no way to enter Setup from this early point during POST.
POST Slow Reboot Cycle	Enable late reboot in POST, allowing service technician to cause the system to move through POST and then reboot, causing POST to be reexecuted, over and over, until Setup is reentered and this option is disabled. When left unattended, this is a straightforward way of having POST exercise system memory and peripherals without requiring a boot to a drive with an operating system installed.

The following table describes the settings associated with the POST setup menu's Device Initialization section:

POST Floppy Seek	Enable head seek on each floppy drive configured in the system. Used to recalibrate the drive in some systems with older DOS operating systems.
POST Hard Disk Seek	Enable head seek on each hard drive configured in the system. This is a way of extending the standard testing performed on each drive during POST, by requesting that the drive actually move the head. Not available with all drives.

B.8 PnP Setup Menu

The PnP menu is used to configure Plug-n-Play, a legacy BIOS initiative used to support operating systems such as Windows95, Windows98, and WindowsNT. ACPI has largely replaced this feature; however, it is necessary for platforms to support older operating systems.



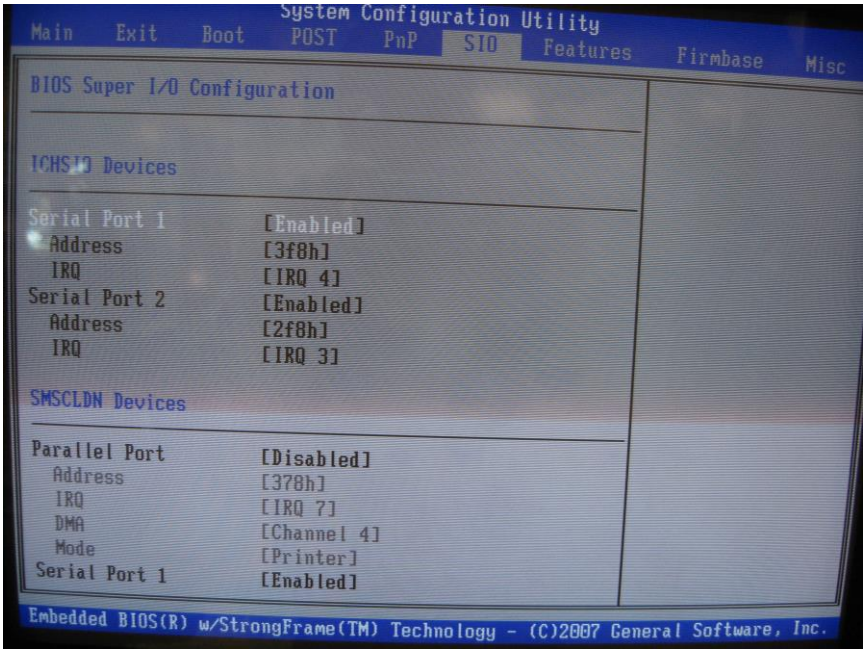
The PnP menu consists of two sections; basic configuration that enables Plug-n-Play and identifies if a PnP should perform configuration or let the OS do it; and then, another section that defines which system IRQs should be reserved for PnP's use, so that PCI doesn't use them. The following table presents the fields in the PnP menu.

Plug-n-Play	Enable PnP feature. When disabled, a PnPaware OS will not find any PnP services in the BIOS, and all other configuration parameters in the menu will be greyed out. Enable to support legacy OSes like DOS, Windows95, Windows98, and WindowsNT. Disable for operating systems like WindowsXP or Windows Vista, or for Linux operating systems with ACPI support.
Plug-n-Play OS	Enable delay of configuration of PnP hardware and option ROMs. When enabled, BIOS will NOT configure the devices, and instead defer assignment of resources, such as DMA, I/O, memory, and IRQs, to the PnP OS. When disabled, the BIOS performs conflict detection and resolution, and assigns resources for the OS. Disable this parameter when running non-PnP OSes like DOS. Enable this parameter when running PnP OSes like Windows95, Windows98, and WindowsNT.
IRQ0	Enable exclusive use of IRQ0 by PnP.
IRQ1	Enable exclusive use of IRQ1 by PnP.
IRQ2	Enable exclusive use of IRQ2 by PnP.
IRQ3	Enable exclusive use of IRQ3 by PnP.
IRQ4	Enable exclusive use of IRQ4 by PnP.
IRQ5	Enable exclusive use of IRQ5 by PnP.
IRQ6	Enable exclusive use of IRQ6 by PnP.
IRQ7	Enable exclusive use of IRQ7 by PnP.
IRQ8	Enable exclusive use of IRQ8 by PnP.
IRQ9	Enable exclusive use of IRQ9 by PnP.

IRQ10	Enable exclusive use of IRQ10 by PnP.
IRQ11	Enable exclusive use of IRQ11 by PnP.
IRQ12	Enable exclusive use of IRQ12 by PnP.
IRQ13	Enable exclusive use of IRQ13 by PnP.
IRQ14	Enable exclusive use of IRQ14 by PnP.
IRQ15	Enable exclusive use of IRQ15 by PnP.

B.9 Super I/O (SIO) Setup Menu

The SIO menu is used to configure the LPC47B27x Super I/O device. The only implemented I/O on this chip are the PS/2 mouse and keyboard and two 2-wire COM ports (COM3 & COM4). Basically this window is used to configure COM3 & COM4 (though they are referred to as Serial Ports 1 & 2 in the SIO Setup Menu):



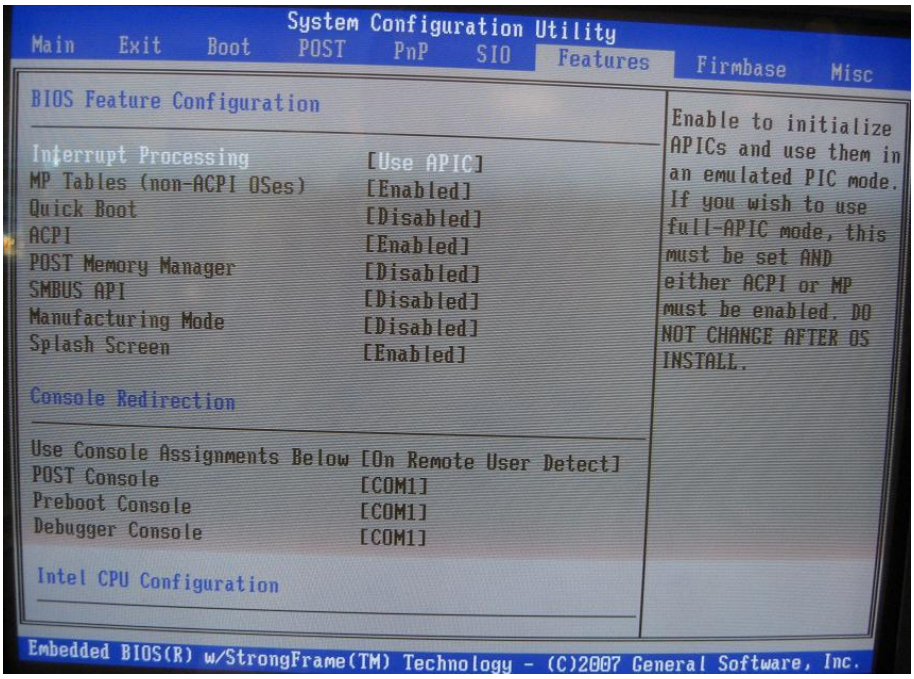
POST reads these settings in the menu shown above and programs the Super I/O part accordingly, enabling and disabling devices as requested. The disabled devices are not further programmed, since they are actually disabled in hardware. In the figure above, legacy I/O addresses and IRQs are as follows:

COM3 – I/O 3f8h, IRQ4.
COM4 – I/O 2f8h, IRQ3.

It should be noted that these are not the only possible addresses, but they are the ones that will ensure compatibility with the most legacy software, especially early DOS programs that do not use BIOS to access the COM ports.

B.10 Features Setup Menu

The Features menu is used to configure the system BIOS' major features, including Quick Boot, APM, ACPI, PMM, SMBUS, SMBIOS, Manufacturing Mode, Splash Screen, Console Redirection, and others added by the OEM. This figure shows a typical Features Setup menu.


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
BIOS Feature Configuration
Interrupt Processing [Use APIC]
MP Tables (non-ACPI OSes) [Enabled]
Quick Boot [Disabled]
ACPI [Enabled]
POST Memory Manager [Disabled]
SMBUS API [Disabled]
Manufacturing Mode [Disabled]
Splash Screen [Enabled]
Console Redirection
Use Console Assignments Below [On Remote User Detect]
POST Console [COM1]
Preboot Console [COM1]
Debugger Console [COM1]
Intel CPU Configuration
Enable to initialize APICs and use them in an emulated PIC mode. If you wish to use full-APIC mode, this must be set AND either ACPI or MP must be enabled. DO NOT CHANGE AFTER OS INSTALL.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

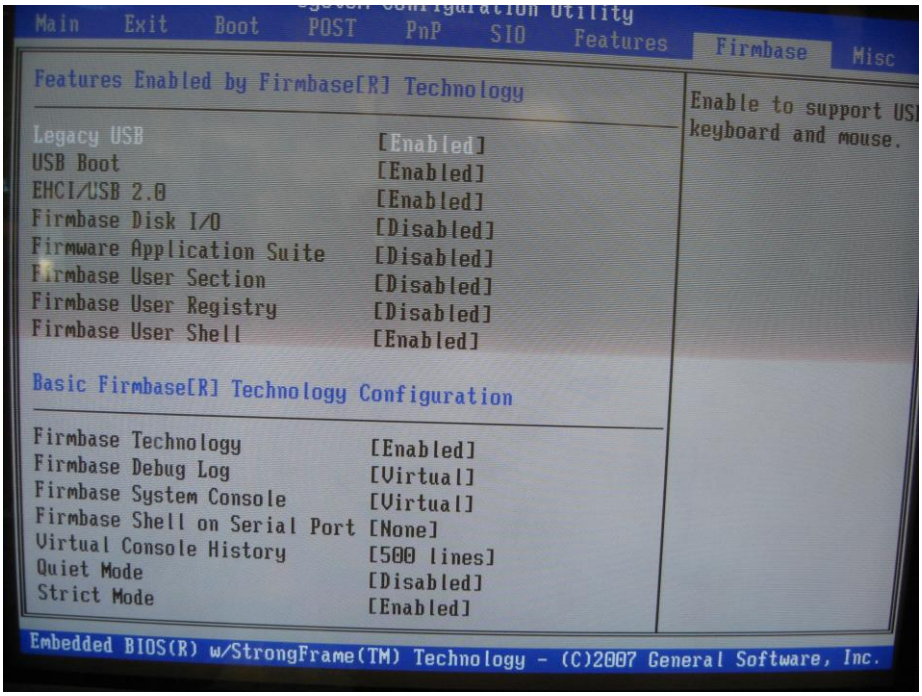
The following table describes each setting in the Features menu :

Quick Boot	Enable time-optimized POST, causing certain preconfigured OEM optimizations to be made when the system boots. Depending on the system, Quick Boot can reach the DOS prompt in as little as 85ms (milliseconds.)
Advanced Power Management (APM)	Enable legacy power management, used by the system when an ACPI-aware operating system is not running (during POST, such as when the system is running the preboot environment, or while running DOS, Windows95, Windows98, or Linux kernels below version 2.6.) Uses the SMM feature (see Firmbase) to operate properly.
ACPI	Enable ACPI system description and power management (ACPI replaces PnP and APM.) Used with ACPI-aware OSes such as Linux kernels version 2.6 and above, Windows XP, and Windows Vista. Commonly also uses the SMM feature (see Firmbase) to operate properly.
POST Memory Manager (PMM)	Enable memory allocation services for option ROMs, especially network cards running PXE. Some option ROMs may use this interface incorrectly, causing system crashes. Other PXE option ROMs may not run if PXE is not supported. Because of the state of these option ROMs, the setting is provided as an option to the user.
SMBUS API	Enable INT 15h services that permit certain software to access devices on the system's SMBUS without having knowledge of the SMBUS controller itself.
System Management BIOS (SMBIOS)	Enable System Management BIOS interface specification support, exposing information about the type of hardware, including the chassis, motherboard layout, type of CPU and DRAM sticks, to applications such as WfM, which runs on PXE in the preboot environment.
Manufacturing Mode	Enable automatic entry into manufacturing mode when POST encounters a critical error. Used in closed device settings such as smart phones that need access to docking stations when they don't boot. Leave disabled.

Splash Screen	Enable graphical POST
Console Redirection	Configure the console redirection feature over a serial port. Automatic – causes POST, the debugger, and the preboot environment to use the system's first serial port (COM1) when an RS232 cable is detected with DSR and CTS modem signals active, indicating a terminal emulation program is likely to be attached to the other end of the cable. Always – causes the BIOS to always use the serial port as the console, without testing for the presence of the terminal emulation program. Never – causes the BIOS to never invoke console redirection, but instead always use the main keyboard and video display. If there is no keyboard or video display, the system operates headless.
EFI Source	Configure the location (ROM or disk) where the EFI boot action can find the EFILDR.BIN image. An image may be merged with the system BIOS into the system ROM, or it may be placed in the root directory of any bootable mass storage device.

B.11 Firmbase Setup Menu

The Firmbase menu configures the Firmbase Technology component of the system BIOS, including all of the features enabled by it; i.e., legacy USB keyboard and mouse, boot from USB devices, and support of Firmbase applications such as Boot Security, Platform Update Facility, and High Availability Monitor. This menu has several parts, with the most basic user oriented feature options in the top section, and the more technical tuning parameters located in the lower sections.


Main Exit Boot POST PnP SIO Features Firmbase Misc
Features Enabled by Firmbase[R] Technology
Enable to support USI keyboard and mouse.
Legacy USB [Enabled]
USB Boot [Enabled]
EHCI/USB 2.0 [Enabled]
Firmbase Disk I/O [Disabled]
Firmware Application Suite [Disabled]
Firmbase User Section [Disabled]
Firmbase User Registry [Disabled]
Firmbase User Shell [Enabled]
Basic Firmbase[R] Technology Configuration
Firmbase Technology [Enabled]
Firmbase Debug Log [Virtual]
Firmbase System Console [Virtual]
Firmbase Shell on Serial Port [None]
Virtual Console History [500 lines]
Quiet Mode [Disabled]
Strict Mode [Enabled]
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The following table presents the settings that enable high-level features enabled by Firmbase Technology:

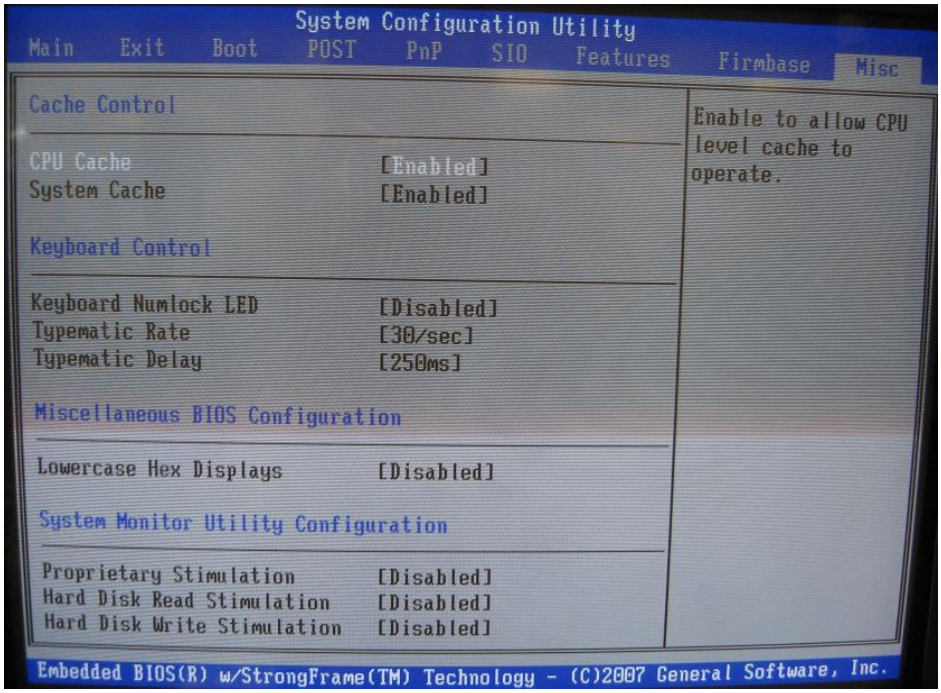
Legacy USB	Enables BIOS support for USB keyboards and mice. Up to 8 USB keyboards and 8 USB mice may be supported at a time. Use of PS/2 keyboard and mouse concurrently with USB devices is discouraged, as the legacy PS/2 keyboard controller cannot easily separate simultaneous data streams from both device classes.
USB Boot	Enables BIOS support for accessing USB mass storage devices and emulating legacy floppy, hard drive, and CDROM drive devices with them. Enable this option in order for USB devices to be supported in the BBS device list(see the BOOT menu.)
EHCI/USB 2.0	Enables EHCI Firmbase Technology driver, allowing USB Boot feature to use high

	speed transfers on USB 2.0 ports in the system.
Firmbase Disk I/O	Enables Firmbase Technology FAT file system driver, so that Firmbase applications such as Boot Security, Platform Update Facility, and HA Monitor, as well as the HA and TCB components of the kerne, have access to files residing on drives containing FAT file systems. Also turn on this option if you wish to run Firmbase applications from FAT file systems on either ATA or USB mass storage devices.
Firmware Application Suite	Enables Firmbase applications configured for the system by the OEM. Typically includes Boot Security, Platform Update Facility, and High Availability Monitor.
Firmbase User Registry	Not used.
Firmbase User Shell	Enables Firmbase Technology command line interpreter, a multi-user command shell with DOS-like and Unix-like command structure;can be used to start Firmbase applications written with the Firmbase SDK, a General Software product.
Firmbase Technology	Enables Firmbase Technology as a whole, the industry's most comprehensive and fullfeatured System Management Mode (SMM) operating environment. Some hardware platforms require Firmbase Technology to run, as they may use it to virtualize hardware such as virtual video and audio PCI devices. Some BIOS features, such as ACPI and APM, may require Firmbase Technology to operate
Firmbase Debug Log	Specifies the device used by Firmbase Technology components (kernel, drivers, and programs) to display debugging instrumentation produced with the dprintf and DPRINTF system functions. None – Instrumentation disabled. COM1 – Write text to 1st serial port. COM2 – Write text to 2nd serial port. COM3 – Write text to 3rd serial port. COM4 – Write text to 4th serial port. Virtual – Write text to virtual console If enabled, this console can provide diagnostic messages (similar to the types displayed by Linux when it boots) for Firmbase Technology features such as USB HID and USB Boot.
Firmbase System Console	Specifies the device used by Firmbase Technology's system process when it initializes the kernel and processes the [SYSTEM] registry section, including its Start and Run commands. None – System console disabled. COM1 – Write text to 1st serial port. COM2 – Write text to 2nd serial port. COM3 – Write text to 3rd serial port. COM4 – Write text to 4th serial port. Virtual – Write text to virtual console If enabled, this console can provide a list of sign-on banners of all Firmbase applications loaded during system initialization.
Firmbase Shell on Serial Port	Specifies a serial port that may be used by Firmbase Technology's command line interpreter as an extra user session for systems that do not have a keyboard or monitor to support virtual consoles. None – Serial console disabled. COM1 – Console on 1st serial port. COM2 – Console on 2nd serial port. COM3 – Console on 3rd serial port. COM4 – Console on 4th serial port.
Virtual Console History	Specifies the number of lines of text that Firmbase Technology maintains in its virtual

	console feature, allowing the user to scrollback through lines previously displayed and scrolled off the screen. OEMs may configure a set of values, such as 20, 50, 100, 200, and 500 lines.
Quiet Mode	Enables a feature that causes the Firmbase kernel to suppress its standard messages to the system console.
Strict Mode	Enables a feature that causes the Firmbase kernel to abort any processes in the system that make software errors in calling system API functions. Examples include blocking at IRQLs other than IRQL_THREAD, or passing a NULL pointer to a C library function that requires a non-NULL pointer, etc. Disabling this feature causes the kernel to skip over the activity that discovered the programming error in the application, allowing it to continue if at all possible, with the consequence that the program may not operate correctly.

B.12 Miscellaneous Setup Menu

The Misc menu provides for configuration of BIOS settings that don't easily fit in any other category. They include Cache Control, Keyboard Control, Debugger Settings, and System Monitor Utility Configuration parameters.


System Configuration Utility
Main Exit Boot POST PnP SIO Features Firmbase Misc
Cache Control
CPU Cache [Enabled]
System Cache [Enabled]
Keyboard Control
Keyboard Numlock LED [Disabled]
Typematic Rate [30/sec]
Typematic Delay [250ms]
Miscellaneous BIOS Configuration
Lowercase Hex Displays [Disabled]
System Monitor Utility Configuration
Proprietary Stimulation [Disabled]
Hard Disk Read Stimulation [Disabled]
Hard Disk Write Stimulation [Disabled]
Enable to allow CPU level cache to operate.
Embedded BIOS(R) w/StrongFrame(TM) Technology - (C)2007 General Software, Inc.

The following table presents the settings in the Misc Setup menu:

System Cache	Enables POST's support for cache in the system. Modern processors virtually require cache to be enabled to achieve acceptable performance. However, to diagnose certain problems related to caching in the system, such as multiprocessing systems, it may be desirable to disable this setting.
Keyboard Numlock LED	Enables the Numlock key when POST initializes the PS/2 keyboard.
Typematic Rate	Specify the rate at which the PS/2 keyboard controller repeats characters when most keys are pressed down. USB typematic is automatic and does not use this parameter.
Typematic Delay	Specifies the amount of time a repeating key may be pressed on a PS/2 keyboard until the key repeat feature begins repeating the keystroke. USB typematic is automatic and does not use this parameter.

Lowercase Hex Displays	Enables the display of hexadecimal numbers in the debugger with lowercase letters instead of uppercase letters (ie, 2f8ah instead of 2F8AH.)
Proprietary Stimulation	Enables System Monitor's callout to the OEM's BPM adaptation code to execute code that causes stimulation of the SMM environment for measurement purposes.
Hard Disk Read Stimulation	Enables System Monitor's read of a preconfigured number of sectors from a location on the first hard disk in the system in order to stimulate the SMM environment. This is useful when measuring code path lengths in USB boot, when the first hard drive is configured in the BBS list as a USB hard drive.
Hard Disk Write Stimulation	Enables System Monitor's write of a preconfigured number of sectors to a location on the first hard disk in the system in order to stimulate the SMM environment. This is useful when measuring code path lengths in USB boot, when the first hard drive is configured in the BBS list as a USB hard drive. Please note that when this parameter is selected, the system automatically enables reading, so that the stimulation of the system includes reading a range of sectors into a memory buffer, and writing the same data back to the same range of sectors for safety. Thus, this feature is theoretically nondestructive. WARNING: YOU ARE ADVISED THAT THIS FEATURE COULD CAUSE DATA LOSS AT YOUR SOLE EXPENSE; ACCORDINGLY, IT IS PROVIDED AS-IS WITHOUT WARRANTY OF ANY KIND. ALWAYS BACKUP YOUR DATA BEFORE PERFORMING DIAGNOSTICS ON ANY SYSTEM, AS THEY COULD CAUSE DATA LOSS.
Floppy Disk Read Stimulation	There is no Floppy Drive interface implemented on the CPU-111-10.

C. Environmental and Power Requirements

The CPU-111-10 power and environmental requirements are shown in the tables below.

The 3 Volt lithium coin cell is a BR1225 with 48 mAhours capacity and it is used to battery-back the Real Time Clock and the BIOS's NV-RAM.

Table 12: Environmental Requirements

Parameter	Condition	Range	Comment
Temperature	Operating	-10˚C to +50˚C	Clock throttling can be implemented for wider temperature ranges
	Storage	-50˚C to +85˚C	
Humidity	Operating	20 to 95% non-condensing	±4% relative humidity, per MIL-STD-810F
	Storage	0 to 100% non-condensing	
Altitude		Unlimited	
Vibration	Sine	10g peak 15-2 kHz	All levels based on a sweep duration of 10 minutes per axis, each of three mutually perpendicular axes. Qualification testing is displacement limited below 44 Hz.
	Random	0.1 g^2/Hz 15-2 kHz ($14.1\ g_{rms}$)	60 minutes per axis each of three mutually perpendicular axes.
	Shock	40 g peak	Three hits per direction per axis, 1/2 sine + terminal peak sawtooth, 11mS (total 36 hits).

Table 13: Power Requirements

Supply Rail	Voltage	Current	Power
VS1, VS2	12V		
VS3	5.0V		

D. RTM Rear Plug-in I/O Expansion Module for the CPU-111-10

Dynatem offers a rear transition module for I/O expansion with the CPU-111-10.

D.1 RTM VPX Pin-outs

Table 14: RTM VPX RP0 Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	No Wafer							
2	Power				No Pad			
3	Power	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)	No Pad	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)
4	Single-ended	RTM_PWREN		GND		GND	SYSRESET#	
5	Single-ended	RTM_MDIO		GND		GND		
6	Single-ended	RTM_MDC		GND		GND		
7	Differential		GND			GND		
8	Differential	GND			GND			GND
9	No Wafer							
10	No Wafer							
11	No Wafer							
12	No Wafer							
13	No Wafer							
14	No Wafer							
15	No Wafer							
16	No Wafer							

Table 15: RTM VPX RP4 Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Differential	COM0-TX	GND	XAUI7-TX0-	XAUI7-TX0+	GND	XAUI7-RX0-	XAUI7-RX0+
2	Differential	GND	XAUI7-TX1-	XAUI7-TX1+	GND	XAUI7-RX1-	XAUI7-RX1+	GND
3	Differential	COM0-RX	GND	XAUI7-TX2-	XAUI7-TX2+	GND	XAUI7-RX2-	XAUI7-RX2+
4	Differential	GND	XAUI7-TX3-	XAUI7-TX3+	GND	XAUI7-RX3-	XAUI7-RX3+	GND
5	Differential		GND	MDX0-A2-	MDX0-A2+	GND	MDX0-B2-	MDX0-B2+
6	Differential	GND	MDX0-C2-	MDX0-C2+	GND	MDX0-D2-	MDX0-D2+	GND
7	Differential	VGA-HS	GND	MDX1-A2-	MDX1-A2+	GND	MDX1-B2-	MDX1-B2+
8	Differential	GND	MDX1-C2-	MDX1-C2+	GND	MDX1-D2-	MDX1-D2+	GND
9	Differential	VGA-VS	GND	SATA0-TX-	SATA0-TX+	GND	SATA0-RX-	SATA0-RX+
10	Differential	GND	SATA1-TX-	SATA1-TX+	GND	SATA1-RX-	SATA1-RX+	GND
11	Differential	VGA-R	GND	SATA2-TX-	SATA2-TX+	GND	SATA2-RX-	SATA2-RX+
12	Differential	GND	SATA3-TX-	SATA3-TX+	GND	SATA3-RX-	SATA3-RX+	GND
13	Differential	VGA-B	GND	SATA4-TX-	SATA4-TX+	GND	SATA4-RX-	SATA4-RX+
14	Differential	GND	SATA5-TX-	SATA5-TX+	GND	SATA5-RX-	SATA5-RX+	GND
15	Differential	VGA-G	GND	USB0-	USB0+	GND	USB1-	USB1+
16	Differential	GND	USB2-	USB2+	GND	USB3-	USB3+	GND

Table 16: RTM VPX RP3 Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Single-ended	J14-1	J14-3	GND	RTM_MDIO	GND	J14-2	J14-4
2	Single-ended	J14-5	J14-7	GND	RTM_MDC	GND	J14-6	J14-8
3	Single-ended	J14-9	J14-11	GND	SMB_B_DAT	GND	J14-10	J14-12
4	Single-ended	J14-13	J14-15	GND	SMB_B_CLK	GND	J14-14	J14-16
5	Single-ended	J14-17	J14-19	GND	RTM_PWREN	GND	J14-18	J14-20
6	Single-ended	J14-21	J14-23	GND	RTM_PWRGD	GND	J14-22	J14-24
7	Single-ended	J14-25	J14-27	GND	EEP_WP	GND	J14-26	J14-28
8	Single-ended	J14-29	J14-31	GND	RTM_PBRST#	GND	J14-30	J14-32
9	Single-ended	J14-33	J14-35	GND		GND	J14-34	J14-36
10	Single-ended	J14-37	J14-39	GND		GND	J14-38	J14-40
11	Single-ended	J14-41	J14-43	GND		GND	J14-42	J14-44
12	Single-ended	J14-45	J14-47	GND		GND	J14-46	J14-48
13	Single-ended	J14-49	J14-51	GND		GND	J14-50	J14-52
14	Single-ended	J14-53	J14-55	GND		GND	J14-54	J14-56
15	Single-ended	J14-57	J14-59	GND		GND	J14-58	J14-60
16	Single-ended	J14-61	J14-63	GND		GND	J14-62	J14-64

Table 17: RTM VPX RP6 Pin-outs

	Wafer Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Single-ended	J24-1	J24-3	GND		GND	J24-2	J24-4
2	Single-ended	J24-5	J24-7	GND		GND	J24-6	J24-8
3	Single-ended	J24-9	J24-11	GND		GND	J24-10	J24-12
4	Single-ended	J24-13	J24-15	GND		GND	J24-14	J24-16
5	Single-ended	J24-17	J24-19	GND		GND	J24-18	J24-20
6	Single-ended	J24-21	J24-23	GND		GND	J24-22	J24-24
7	Single-ended	J24-25	J24-27	GND		GND	J24-26	J24-28
8	Single-ended	J24-29	J24-31	GND		GND	J24-30	J24-32
9	Single-ended	J24-33	J24-35	GND		GND	J24-34	J24-36
10	Single-ended	J24-37	J24-39	GND		GND	J24-38	J24-40
11	Single-ended	J24-41	J24-43	GND		GND	J24-42	J24-44
12	Single-ended	J24-45	J24-47	GND		GND	J24-46	J24-48
13	Single-ended	J24-49	J24-51	GND		GND	J24-50	J24-52
14	Single-ended	J24-53	J24-55	GND		GND	J24-54	J24-56
15	Single-ended	J24-57	J24-59	GND		GND	J24-58	J24-60
16	Single-ended	J24-61	J24-63	GND		GND	J24-62	J24-64

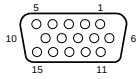
D.2 CPU-111-10 Rear Transition Module PMC I/O Pin-outs

Table 18: PMC I/O Header Pin-outs

J2				J4				J1				J3			
63	J14-64	GND	64	63	J14-63	GND	64	63	J24-64	GND	64	63	J24-63	GND	64
61	J14-62	GND	62	61	J14-61	GND	62	61	J24-62	GND	62	61	J24-61	GND	62
59	J14-60	GND	60	59	J14-59	GND	60	59	J24-60	GND	60	59	J24-59	GND	60
57	J14-58	GND	58	57	J14-57	GND	58	57	J24-58	GND	58	57	J24-57	GND	58
55	J14-56	GND	56	55	J14-55	GND	56	55	J24-56	GND	56	55	J24-55	GND	56
53	J14-54	GND	54	53	J14-53	GND	54	53	J24-54	GND	54	53	J24-53	GND	54
51	J14-52	GND	52	51	J14-51	GND	52	51	J24-52	GND	52	51	J24-51	GND	52
49	J14-50	GND	50	49	J14-49	GND	50	49	J24-50	GND	50	49	J24-49	GND	50
47	J14-48	GND	48	47	J14-47	GND	48	47	J24-48	GND	48	47	J24-47	GND	48
45	J14-46	GND	46	45	J14-45	GND	46	45	J24-46	GND	46	45	J24-45	GND	46
43	J14-44	GND	44	43	J14-43	GND	44	43	J24-44	GND	44	43	J24-43	GND	44
41	J14-42	GND	42	41	J14-41	GND	42	41	J24-42	GND	42	41	J24-41	GND	42
39	J14-40	GND	40	39	J14-39	GND	40	39	J24-40	GND	40	39	J24-39	GND	40
37	J14-38	GND	38	37	J14-37	GND	38	37	J24-38	GND	38	37	J24-37	GND	38
35	J14-36	GND	36	35	J14-35	GND	36	35	J24-36	GND	36	35	J24-35	GND	36
33	J14-34	GND	34	33	J14-33	GND	34	33	J24-34	GND	34	33	J24-33	GND	34
31	J14-32	GND	32	31	J14-31	GND	32	31	J24-32	GND	32	31	J24-31	GND	32
29	J14-30	GND	30	29	J14-29	GND	30	29	J24-30	GND	30	29	J24-29	GND	30
27	J14-28	GND	28	27	J14-27	GND	28	27	J24-28	GND	28	27	J24-27	GND	28
25	J14-26	GND	26	25	J14-25	GND	26	25	J24-26	GND	26	25	J24-25	GND	26
23	J14-24	GND	24	23	J14-23	GND	24	23	J24-24	GND	24	23	J24-23	GND	24
21	J14-22	GND	22	21	J14-21	GND	22	21	J24-22	GND	22	21	J24-21	GND	22
19	J14-20	GND	20	19	J14-19	GND	20	19	J24-20	GND	20	19	J24-19	GND	20
17	J14-18	GND	18	17	J14-17	GND	18	17	J24-18	GND	18	17	J24-17	GND	18
15	J14-16	GND	16	15	J14-15	GND	16	15	J24-16	GND	16	15	J24-15	GND	16
13	J14-14	GND	14	13	J14-13	GND	14	13	J24-14	GND	14	13	J24-13	GND	14
11	J14-12	GND	12	11	J14-11	GND	12	11	J24-12	GND	12	11	J24-11	GND	12
9	J14-10	GND	10	9	J14-9	GND	10	9	J24-10	GND	10	9	J24-9	GND	10
7	J14-8	GND	8	7	J14-7	GND	8	7	J24-8	GND	8	7	J24-7	GND	8
5	J14-6	GND	6	5	J14-5	GND	6	5	J24-6	GND	6	5	J24-5	GND	6
3	J14-4	GND	4	3	J14-3	GND	4	3	J24-4	GND	4	3	J24-3	GND	4
1	J14-2	GND	2	1	J14-1	GND	2	1	J24-2	GND	2	1	J24-1	GND	2

D.3 Rear Panel Connector Pin-outs

Table 19: RTM Rear Panel Connector Pin-outs

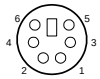


VGA Connector

Pin	Signal
1	VGA_RED
2	VGA_GREEN
3	VGA_BLUE
4	
5	GND
6	GND
7	GND
8	GND
9	5V
10	GND
11	
12	
13	VGA_HS
14	VGA_VS
15	

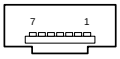
USB Connectors

Pin	Signal
1	5V
2	USB-
3	USB+
4	GND



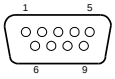
PS2 Connector

Pin	Signal
1	KYBD_DATA
2	M_DATA
3	GND
4	KYBD_VCC
5	KYBD_CLK
6	M_CLK



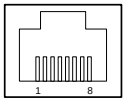
SATA Connectors

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



SERIAL PORT

Pin	Signal
1	
2	RX+
3	TX+
4	
5	GND
6	RX-
7	
8	
9	TX-



Ethernet Connectors

Pin	Signal
1	MX1+
2	MX1-
3	MX2+
4	MX3+
5	MX3-
6	MX2-
7	MX4+
8	MX4-